Assignment 3

ELE-350: Digital Electronics

Winter 2001

Name: _____ **ID:** _____

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1. Draw the circuit diagram that would be implemented by this code segment.

```
input x; reg [5:0] G;
always @(posedge clk)
   G <= {G[4:0], G[5]^x};
```

2. What function does this code segment represent?

```
output out;
input i0, i1, i2, i3;
input s1, s0;
assign out = s1 ? (s0 ? i3 : i2) : (s0 ? i1 : i0);
```

Replace the *assign* statement with a more readable one (still one line).

3. Write the full Verilog code for a 4-bit ripple counter using toggle flip-flops. The counter has an asynchronous reset and a terminal-count output. The cell library doesn't have toggle flip-flops.