Assignment 2

ELE-350: Digital Electronics

Winter 2001

Name: _____ **ID:** _____

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1. Implement the equation $X = ((\bar{A} + \bar{B})(\bar{C} + \bar{D} + \bar{E}) + \bar{F})\bar{G}$ using conventional CMOS technique.

a. Verify your implementation using Demorgan's theorem. [1]

b. You realize that there are more than one way of arranging the transistors for this same function. Suggest a topology (i.e. arrangement or configuration) that gives you the lowest delay and a topology that gives you the highest delay. Explain why in each case. [2]

c. Size the devices such that the output resistance is the same as that of an inverter with NMOS W/L=1 and PMOS W/L=3.

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[1] Answer: $\bar{X} = ((AB + CDE)F) + G$.

[2] Hint: delay is a function of resistance (i.e. current and voltage) and capacitance. The most important capacitances are those at the inputs and the output of a logic gate, because they see the full voltage swing across them. The internal node capacitances only see a partial voltage swing across and, thus, are usually ignored in hand calculations.

2. Assume that the logic gate of Problem 1 with the "lowest delay" topology is connected to an inverter of size NMOS W/L=1 and PMOS W/L=3. The following data are given. [3]

NMOS transistor data: L = 1.2 μm, V_{TO}=0.74 V, k' = 19.6 $\times$ 10^{-6} A/V^2, λ=0.06 V^{-1}, C_{gdo}=0.43 fF/μm, C_j=0.3 fF/μm, C_{jsw}=0.8 fF/μm, t_{ox}=200E-10 m, and from layout assume: AD=10 μm^2, PD=15 μm, AS=10 μm^2, PS=15 μm.

PMOS transistor data: L = 1.2 μm, V_{TO}=-0.74 V, k' = 5.4 $\times$ 10^{-6} A/V^2, λ=0.19 V^{-1}, C_{gdo}=0.43 fF/μm, C_j=0.5 fF/μm, C_{jsw}=0.135 fF/μm, t_{ox}=200E-10 m, and from layout assume: AD=30 μm^2, PD=40 μm, AS=30 μm^2, PS=40 μm.

General data: V_{DD}=3 V, all m=0.5 (abrupt junction), ϕ_0=0.6 V, ε_{ox}=3.5 E-13 F/cm.

a) Calculate the falling, rising, and average delays from the input of the logic gate to the input of the inverter. Ignore all internal node capacitances and assume that the relevant transistors operate in saturation during transition to $V_{DD}/2$. Use the average current formula.

b) Repeat (a) using the RC delay formula. Are the answers close to those of part (a)?

b) Calculate the dynamic energy dissipation per cycle. Again ignore the internal capacitances.

[3] Sorry, no answers. I may put them later.