Midterm Exam, Winter 2005, February 28

ELEC-3500: Digital Electronics

Department of Electronics, Carleton University

Instructor: Maitham Shams **Name:** _____

Aids: Closed Book **ID:** _____

Q1	Q2	Q3	Total
/20	/30	/50	/100

Write your name and ID number on all pages. There are three questions. Read the instructions here and for each question carefully to avoid regrets!

- You have *one hour* to write the exam. No questions answered *at all*.
- If you are asked to make an assumption, then you **must** use it, but only for that particular question. State and justify any additional assumptions you make in a question.
- After marking, exam papers are copied in random before returning to students. Students who want their papers to be remarked, **must** hand in the papers to the instructor by the end of the class or lab section in which they get their marked papers back.

Formula

$$
\begin{aligned}
C_{ox} &= \frac{\varepsilon_{ox}}{t_{ox}} \\
C_j &= \frac{C_{j0}}{(1 - V_D/\phi_0)^m} \\
K_{eq} &= \frac{-\phi_0^m}{(V_H - V_L)(1-m)}[(\phi_0 - V_H)^{1-m} - (\phi_0 - V_L)^{1-m}] \\
V_T &= V_{T0} + \gamma(\sqrt{|\, -2\phi_F + V_{SB}\,|} - \sqrt{|\, -2\phi_F\,|}) \\
I_D(\text{sat}) &= \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \\
I_D(\text{linear}) &= k'\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)
\end{aligned}
$$

Data

NMOS: $L = 0.5$ μm, V_{TO}=0.6 V, $k' = 40 \times 10^{-6}$ A/V^2, λ=0 V^{-1}, C_j=0.5 fF/μm^2, C_{jsw}=0.3 fF/μm, t_{ox}=150E-10 m.

PMOS: $L = 0.5$ μm, V_{TO}=-0.7 V, $k' = 15 \times 10^{-6}$ A/V^2, λ=0 V^{-1}, C_j=0.5 fF/μm^2, C_{jsw}=0.3 fF/μm, t_{ox}=150E-10 m.

General: m=0.5 (abrupt junction), ϕ_0=0.6 V, ε_{ox}=3.5 E-13 F/cm.

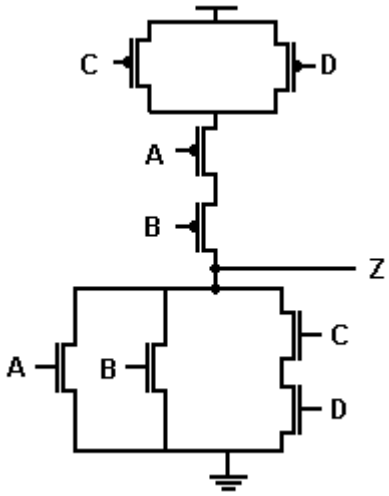
[1] (20 marks) Implement the following function in CMOS. Do not use over *eight* transistors in your implementation.

$Z = \overline{A + B + CD}$

$Z = \overline{A} \cdot \overline{B} \cdot \overline{CD}$

$Z = \overline{A} \cdot \overline{B} \cdot (\overline{C} + \overline{D})$

$\overline{Z} = A + B + CD$



[1] (30 marks) Circle True (T) or false (F)?

- (T / F) Threshold voltage of NMOS transistor increases as sourse-to-body potential increases.**True**
- (T / F) CMOS means Conventional Metal-Oxide-Semiconductor.**False**
- (T / F) When the input signal voltage of an inverter is between V_{IL} and V_{IH}, the output is in a stable logic state.**False**
- (T / F) The resistance of two similarly sized (W, L) MOS transistors in series is like the resistnce of a single transistor with half of the size (W/2, L).**True**
- (T / F) A CMOS NAND gate is larger than an equally fast NOR gate.**False**
- (T / F) In standard CMOS, only inverted functions of primary inputs can be implemented in one stage (i.e. one logic gate).**True**
- (T / F) "always (posedge ...)" produces one or more flipflops. **True**

- (T / F) A "reg z" declaration must produce a register for z. **False**
- (T / F) All "assignment" statements in structural Verilog run in parallel. **True**
- (T / F) Frequency of oscillation of a closed-loop chain of similarly sized CMOS inverters is independent of the size. **True**

[3] (50 marks) Design a CMOS NAND gate with symmetric response to drive a bus capacitive load of 1 pF with a rising and falling propagation delay of 0.5 ns each. The supply voltage is 3 volts. Assumptions: a) transistors operate in saturation during transitions, b) ignore the diffusion capacitances and the internal capacitances, c) channel-length modulation factor is zero. Find the following:
i)Dynamic Energy dissipation per cycle due to output (bus only).
ii)Static Energy dissipation per cycle.
iii)Size of NMOS transistor.
iv)Size of PMOS transistor.
v)Power dissipation at maximum frequency of operation.
vi)If you use a 2 v power supply instead, how much do you gain in (reducing) Energy consumption and how much do you lose in speed (delay)?

i) $E_D = CV_{DD}^2 = 1 \times 9 = 9pJ$

ii) $E_S = 0$

iii) $D_f = \frac{CV_{DD}}{2In}$, $0.5ns = \frac{CV_{DD}}{2\frac{Kn}{2}\frac{W_n}{L}(V_{DD}-V_{Tn})^2}$, $L = 0.5um, W_n = 13um$

iv) $D_r = \frac{CV_{DD}}{2Ip}$, $0.5ns = \frac{CV_{DD}}{2\frac{Kp}{2}\frac{W_p}{L}(V_{DD}-V_{Tp})^2}$, $L = 0.5um, W_p = 38um$

v) $f_{max} = \frac{1}{2D} = \frac{1}{0.5n\times 2} = 1GHz$, $P = CV_{DD}^2 f_{max} = 9mW$

vi) $\frac{E'}{E} = \frac{CVDD^2}{CV_{DD}^2} = \frac{4}{9} = 44\%$, we reduce energy by 5pJ or energy is less than half.

$\frac{D_f'}{D_f} = \frac{C'V_{DD}'[2\frac{K_n}{2}\frac{W_n}{L}(V_{DD}'-V_{Tn})^2]}{CV_{DD}[2\frac{K_n}{2}\frac{W_n}{L}(V_{DD}-V_{Tn})^2]} = \frac{V_{DD}'(V_{DD}-V_{Tn})^2}{V_{DD}(V_{DD}'-V_{Tn})^2} = 1.95,\ D_f' = 0.98ns.$

$\frac{D_r'}{D_r} = \frac{V_{DD}'(V_{DD}-V_{Tp})^2}{V_{DD}(V_{DD}'-V_{Tp})^2} = 2.09,\ D_r' = 1.04ns.$

$D' = \frac{(D_r'+D_f')}{2} = 1.01$, delay almost doubles.

[4] (50 marks) Write a Verilog code for a T-flipflop (Tff). This flipflop has an input T and an output Q. With each positive edge of clock (clk), the output (Q) is inverted if the input (T), is logic "1"; and the output (Q) doesn't change if the input (T) is logic "0". The flipflop has an asynchronous positive edge reset (rst). Only use the given inputs and outputs (T, Q, clk, rst).

module Tff (Q, T, clk, rst)
input T, clk, rst;
output Q;

write T, clk, rst;
reg Q;

always @(posedge clk or posedge rst)
if (rst) Q ¡= 0;
elseif (T) Q ¡= Q;
endmodule

Bonus (10 marks)

Draw the circuit that is going to be produced from the code (the right code of course).