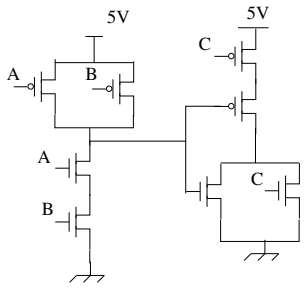
ELEC 3500: Midterm Winter 2005

Duration: 1 hr 15 mins Max Marks: 25

*Answer all **five** questions. Non-programmable calculators are allowed. Answer all questions on the answer script provided to you. If you have any concern with a question in the exam, make any assumption that you think is right and state the assumption clearly on your answer script. Best of luck!!*

1. Implement $F = \overline{\overline{AB} + C}$ using CMOS logic. (Use max 8 transistors) 5 marks

   Ans:



2. Find the rise time (t_r^{nand}) of a three input CMOS Nand gate in terms of the rise time (t_r^{inv}) of a CMOS inverter. The drain capacitor of the PMOS transistor is C and the drain capacitor of the NMOS transistor can be neglected. Also neglect the load capacitance. Channel resistance of both PMOS and NMOS transistors is given as R. (Don't just write down the answer, show the working) 5 marks

   Ans: $t_r^{nand} = [1-3]t_r^{inv}$

3. Registers `x` and `y` are declared as `reg [2:0] x,y;`. `x` and `y` have initial values of 1 and 2 respectively. Find the value of `x` and `y` after each of the following Verilog codes have been executed. 5 marks

   (a)
   ```
   y = x && y;
   x = y & x;
   ```
   Ans: x = 1, y = 1

   (b)
   ```
   x <= (y) ? y : x;
   y <= (x) ? x : y;
   ```
   Ans: x = 2, y = 1

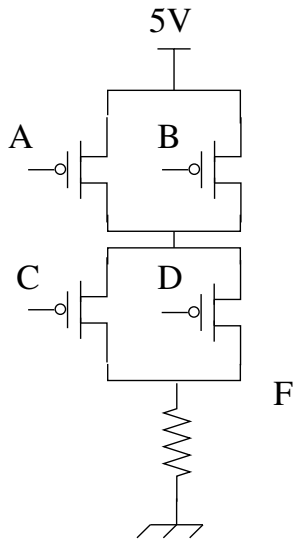
   (c)
   ```
   x = (y) ? y : x;
   y = (x) ? x : y;
   ```
   Ans: x = 2, y = 2

   (d)
   ```
   x <= x << 1;
   x[0] <= x[2];
   ```
   Ans: x = 2, y = 2

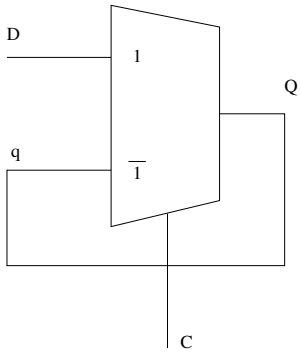
   (e)
   ```
   x = x && (~y);
   y = x + y;
   ```
   Ans: x = 1, y = 3

4. Implement $F = \overline{AB + CD}$ using PMOS logic. 5 marks

   Ans:



5. A d-latch is implemented as shown in the following figure. The mux is implemented using pass-transistors.
5 marks



(a) Will this circuit function properly as a d-latch? Support your answer with justification.
Ans: This will not work properly as a d-latch because there is no energy flowing into the feedback loop.

(b) If your answer in (a) is “no” then modify the circuit to make it work. Show the modified circuit.
Ans: This problem can be addressed by adding a buffer in the feedback loop.