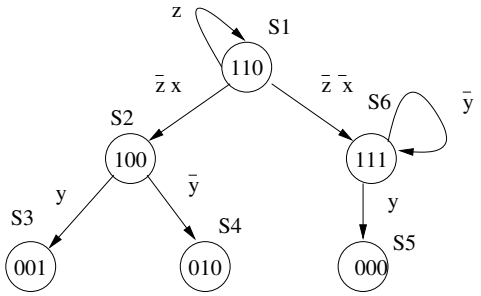
ELEC 3500: Assignment 4

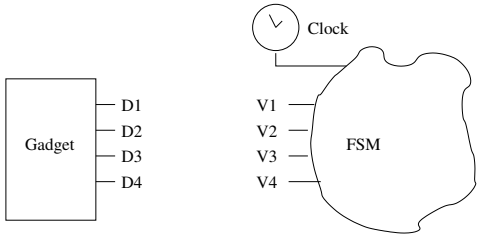
Due on 6th Apr 2005 in class. Total marks: 20

1. The state diagram shown below describes a synchronous FSM with inputs x, y and z. z is a synchronous signal wheras x and y are asynchronous. Is there a problem with this design? If so, suggest a solution to the problem. 5 Marks

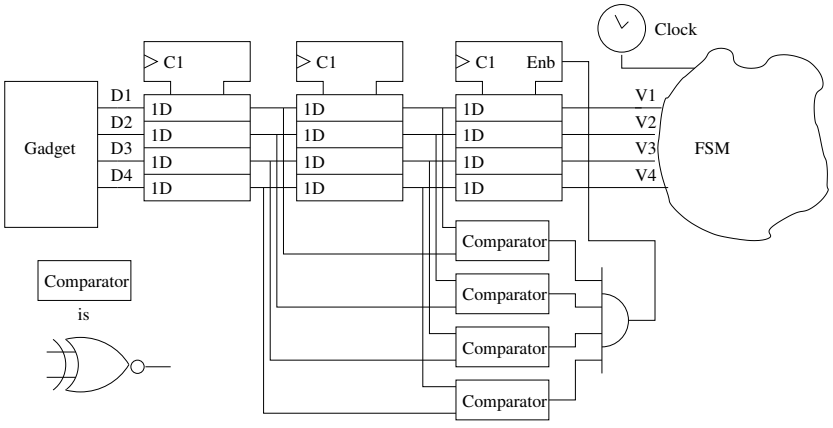


Ans: Make S2 and S6 differ by one bit; S3 and S4 differ by one bit; S6 and S5 differ by one bit.

2. Interface the gadget with the FSM shown in the following figure using debouncing. 3 Marks

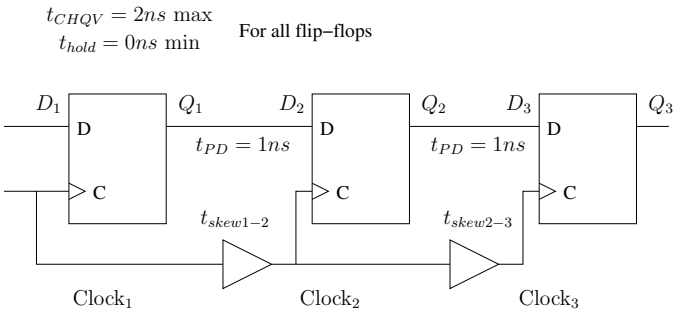


Ans:



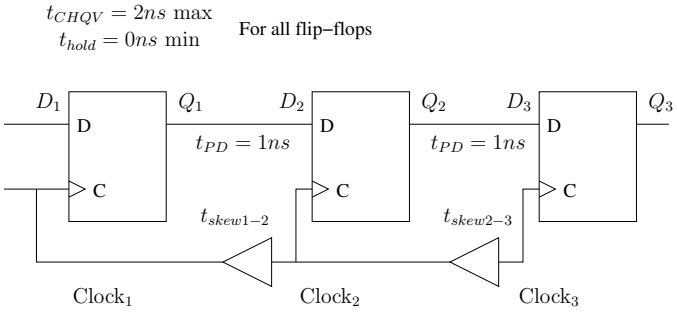
3. Find the maximum delay in the clock buffers for the shift registers shown. $t_{clk} = 10ns$

(a) 2 Marks



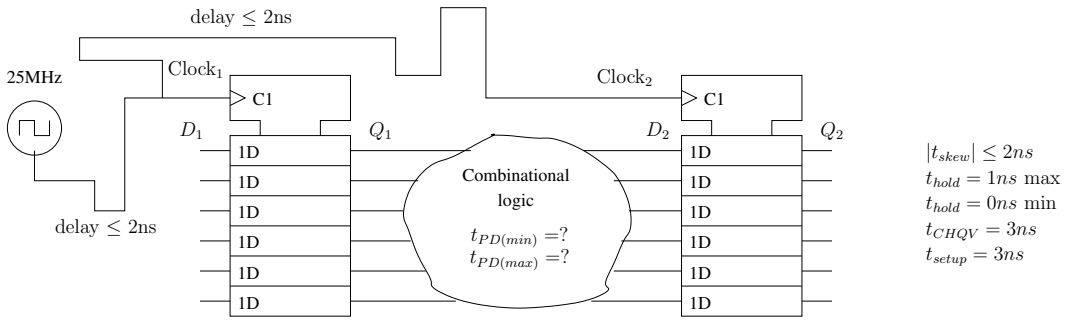
Ans: $t_{PD} \geq t_{hold} + t_{skew} - t_{CHQV} \implies 1 \geq 0 + t_{skew1-2} - 2$ and $1 \geq 0 + t_{skew2-3} - 2$. Hence, $t_{skew1-2} \leq 3ns$ and $t_{skew2-3} \leq 3ns$

(b) 2 Marks



Ans:$t_{skew1-2} \leq t_{clk} = 1ns$ and $t_{skew2-3} \leq t_{clk} = 1ns$

4. Find $t_{PD(min)}$ and $t_{PD(max)}$ in the following circuit. 4 Marks



Ans: $t_{PD(min)} = t_{hold} + |t_{skew}| - t_{CHQV}$ so $t_{PD(min)} = 1 + 2 - 3 = 0ns$. $t_{PD(max)} = t_{clk} - |t_{skew}| - t_{setup} - t_{CHQV}$ so $t_{PD(max)} = 40 - 2 - 3 - 3 = 32ns$

5. (a) An asynchronous signal is synchronized through a single D flip-flop before being fed directly to a flip-flop in a synchronous FSM. The system is clocked at a frequency of 20MHz and the average data frequency is 1MHz. The rise time of the data signal is 1ms. The setup time of the signal is 30ns and the τ of the D latches is given to be 0.43ns. Calculate MTBF. 2 Marks

Ans:

$$MTBF = \frac{e^{T_J/\tau}}{K \cdot f_C \cdot f_D}$$

$K = 2t_{rise}, T_J = T_{CLK} - T_{setup} = 50ns - 30ns = 20ns$. MTBF can be evaluated to be 3.96×10^9.

(b) In the above question instead of using one flip-flop for synchronization, two flip-flops are used for synchronization. In addition, a digital gate is introduced between the synchronization block and the FSM. The digital gate has a propagation delay of 10ns. Calculate MTBF. 2 Marks

Ans:

$T_J = 2T_{CLK} - T_{prop-delay} - 2T_{setup} = 2 * 50ns - 10ns - 2 * 30ns = 30ns$. MTBF can be evaluated to be 4.98×10^{19}.