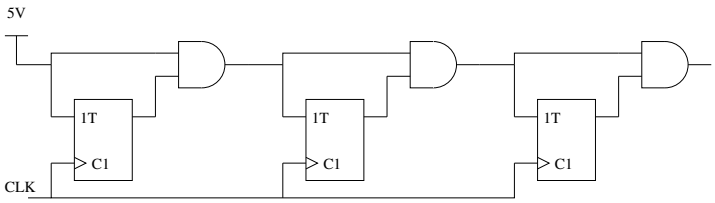
ELEC 3500: Assignment 3 - Solutions

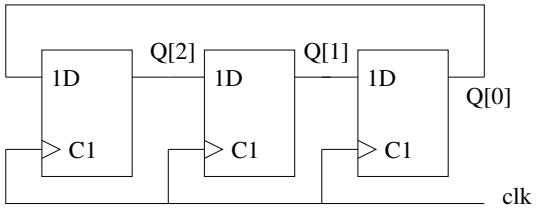
Due on 23rd Mar 2005 in class. Total marks: 20

1. Draw the gate-level circuitry for a 3-bit binary up counter. (You don't have to break down the flip-flips to gate level) 2 marks

   Ans:



2. Write the Verilog code to implement the following shift register. 2 marks



   Ans:

```
module shftreg1(Q, d, clk);
input clk, d;
output [2:0] Q;
reg [2:0] Q;

always @(posedge clk)
begin
   Q<=Q>>1;
   Q[2]<=Q[0];
end
endmodule
```

3. (a) A Mobius counter has 5 flip-flops. How many states will this counter have. 1 mark

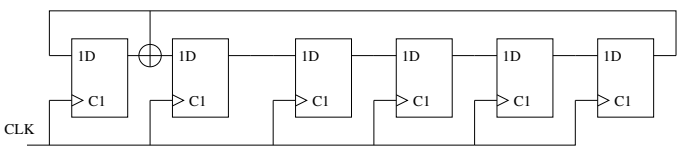
   Ans: 10 states

   (b) The output of a Mobius counter running on a fast clock is interfaced with a synchronous circuit with a slower clock. Would there be a problem with this set-up. Justify your answer. 1 mark

   Ans: Yes. The output of the Mobius counter is asynchronous with respect to the circuit with a slower clock. It has to be synchronized before being fed to a circuit with a slower clock.

4. (a) Draw the LFSR (with internal circuit) corresponding to the polynomial $1 + X + X^6$. (assume naming convention from left to right as discussed in class) 1 mark

   Ans:



(b) Draw the state diagram for this LFSR indicating the value stored in the counter at each stage. 3 marks

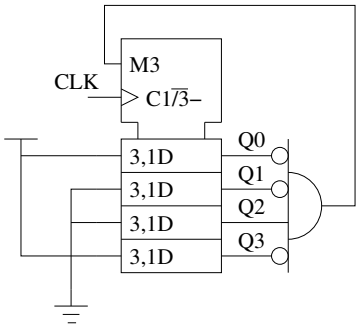
Ans: 100000 → 010000 → 001000 → 000100 → 000010 → 000001 → 110000 → 011000 → 001100 → 000110 → 000011 → 110001 → 101000 → 010100 → 001010 → 000101 → 110010 → 011001 → 111100 → 011110 → 001111 → 110111 → 101011 → 100101 → 100010 → 010001 → 111000 → 011100 → 001110 → 000111 → 110011 → 101001 → 100100 → 010010 → 001001 → 110100 → 011010 → 001101 → 110110 → 011011 → 111101 → 101110 → 010111 → 111011 → 101101 → 100110 → 010011 → 111001 → 101100 → 010110 → 001011 → 110101 → 101010 → 010101 → 111010 → 011101 → 111110 → 011111 → 111111 → 101111 → 100111 → 100011 → 100001 → 100000

(c) Based on the state-diagram from (b) comment on whether $1 + X + X^6$ is a primitive or non-primitive polynomial. 1 mark

Ans: Number of distinct states is $63 = 2^6 - 1$. Hence $1 + X + X^6$ is a primitive polynomial.

5. Design a counter that counts from 9 to 4. Draw the schematic. 2 marks

Ans:



6. Write down the values that a 5 bit ripple counter would take during a transition from 15 to 16. 2 marks

Ans: 01111 → 01110 → 01100 → 01000 → 00000 → 10000

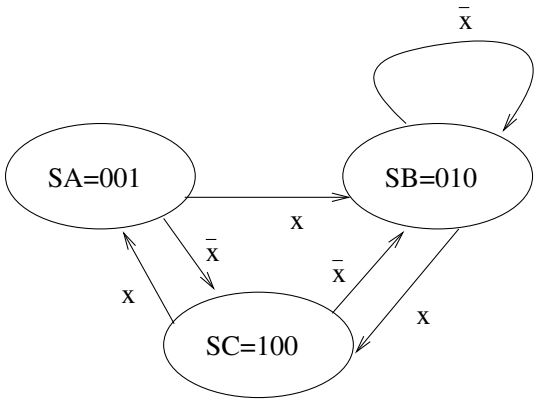
7. Write the Verilog code to implement a 2-bit Gray code counter using look-up tables. 2 marks

Ans:

```
module gray(Q, reset, clk);
input clk, reset;
output [1:0] Q;
reg [1:0] Q;

always @(posedge reset or posedge clk)
if (reset)
   Q <= 0;
else
   case (Q)
      2'b00: Q <= 2'b01
      2'b01: Q <= 2'b11
      2'b11: Q <= 2'b10
      2'b10: Q <= 2'b00
      default: Q <= 2'bxx
   endcase
```

8. Consider the following FSM. Let the present state be represented by CBA and the next-state be represented by $c^+b^+a^+$. Find c^+, b^+ and a^+ in terms of A, B, C and x by inspection. 3 marks



Ans: $a^+ = xC; \quad b^+ = xA + \bar{x}B + \bar{x}C; \quad c^+ = \bar{x}A + xB$