

ELEC 3500: Assignment 2 Solutions

1. State whether the following Verilog procedures generate combinational logic, latches or flip-flops. If a procedure generates latches, modify the code to produce combinational logic. 8 Marks
For marking: Questions (a) and (f) do not contain latches. They carry 1 mark each. The other questions contain latches. They carry two marks. Identification of latches carries one mark and eliminating them by modification of the code carries another mark.

(a) wire A, B;
reg Y;

```
always @(A or B)
begin
    Y = A|B;
end
```

Ans: Combinational Logic

(b) wire A, B, C;
reg Y;

```
always @(A or B)
begin
    Y = (A|B)&C;
end
```

Ans: Produces latches. Modify the code by adding C to the trigger list. `always @(A or B or C)`

(c) reg s;
reg q,r;

```
always @(s)
begin
    case (s)
        1'b0: q = 1'b1;
        1'b1: r = 1'b1;
    endcase
end
```

Ans: Produces latches. Modify the code to initialize q and r before the case statement eg. `q=0;r=0;`. Or make sure that both q and r are given values in both paths of the case statement.

(d) reg [1:0] x;
reg [1:0] q;

```
always @(x)
begin
    case (x)
        2'b00: q = 2'b01;
        2'b10: q = 2'b10;
    endcase
end
```

Ans: Produces latches. Adding a default case for the case statement eliminates the latches.
`default: q = 2'b00;`

(e) wire A, D;
reg B, C, D;

```
always@(posedge A)
begin
    B <= C;
    C <= D;
```

end

Ans: Produces flip-flops.

2. Registers a, b are declared as `reg [2:0] a, b;`. a and b have initial values of 3 and 1 respectively. Find the values of a and b after each of the following Verilog codes are executed. 6 Marks

- (a) `a = b + 2;`
`b = a + 2;`
Ans: a = 3; b = 5;
- (b) `b = a + 2;`
`a = b + 2;`
Ans: a = 7; b = 5;
- (c) `a <= b + 2;`
`b <= a + 2;`
Ans: a = 3; b = 5;
- (d) `b <= a + 2;`
`a <= b + 2;`
Ans: a = 3; b = 5;
- (e) `b = a && b;`
`a = b & a;`
Ans: a = 1; b = 1;
- (f) `a <= |b;`
`b <= &a;`
Ans: a = 1; b = 0;

3. Draw the state diagram of the FSM implemented by the following Verilog code. 2 Marks

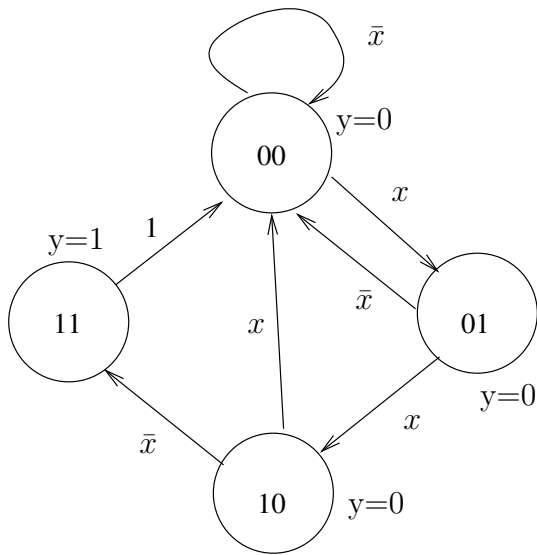
```
reg [1:0] a,b;
wire x,y;

always @(a or x)
begin
    case (a)
        2'b00: b = (x) ? 2'b01 : 2'b00;
        2'b01: b = (x) ? 2'b10 : 2'b00;
        2'b10: b = (!x) ? 2'b11 : 2'b00;
        2'b11: b = 2'b00;
    endcase
end

always @(posedge clk)
begin
    a <= b;
end

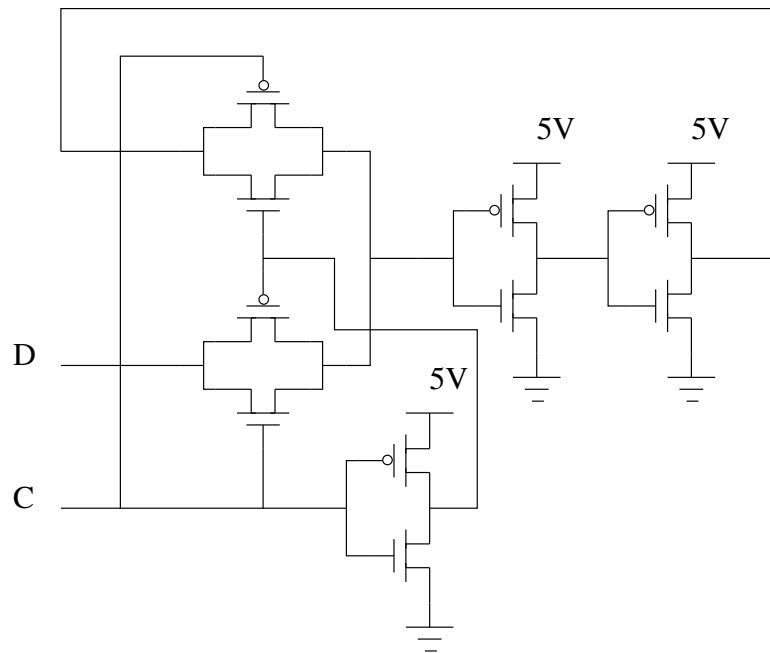
assign y = &a;
```

Ans:



4. Draw the transistor level circuitry using CMOS logic for a functional D-latch constructed using a Mux. The Mux is implemented using pass transistors. 2 marks

Ans:



5. (a) What is wrong with the following circuit? 1 mark

Ans: The clock is gated. It will create a clock skew.

(b) Suggest a cure.

1 mark

Ans: Use an enabled D flip-flop.

