Custom Circuit Design

Handcrafted circuits for high performance & integration density

- Labor intensive
- Expensive
- Long time-to-market

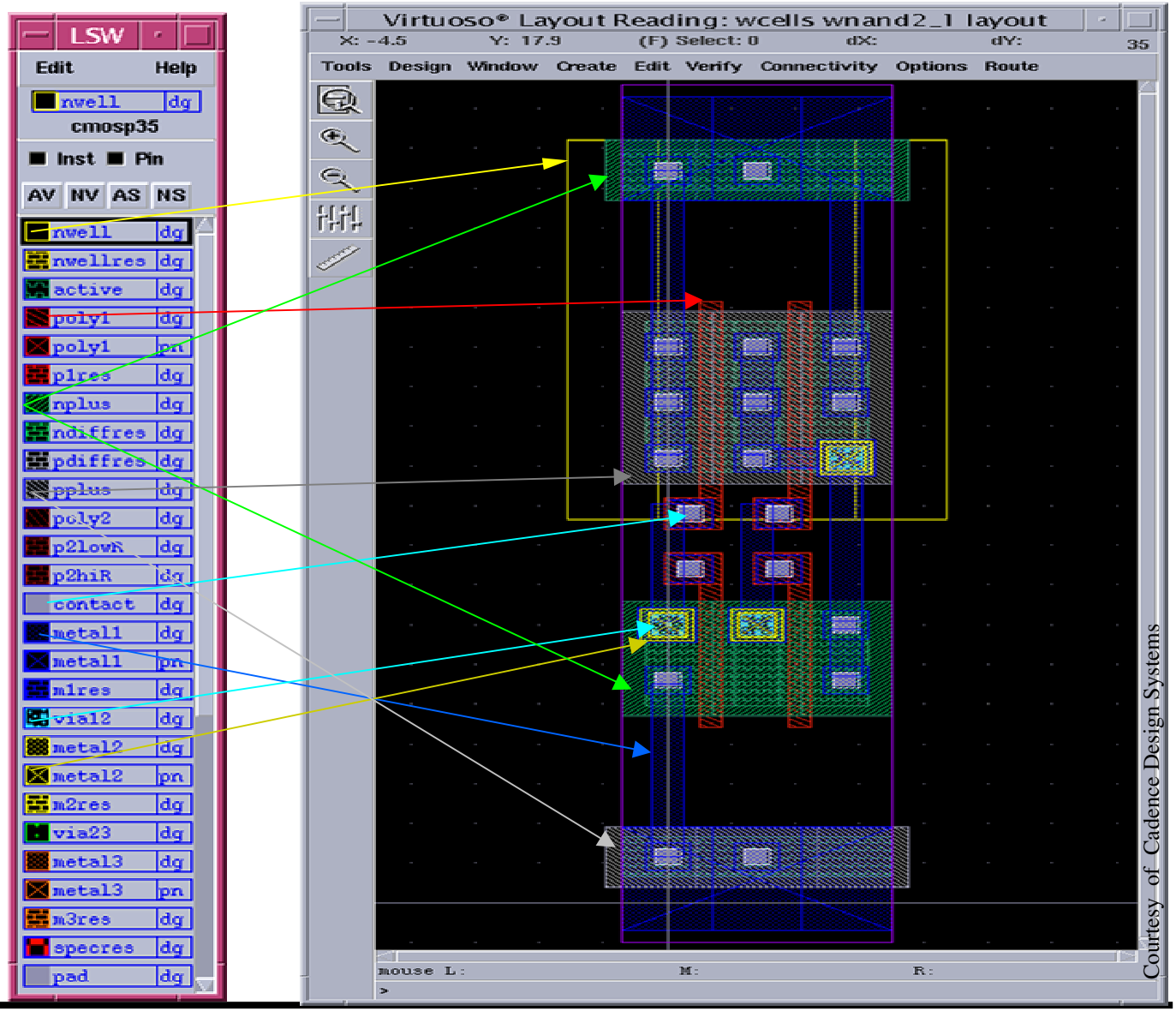
Reasons for Custom circuit design

Cost amortization over large volume, like microprocessors and memory

Extensive reuse of block, like library cell

Cost is not a primary concern (i.e. I don't care, I am RICH), like space applications

- Need a layout editor



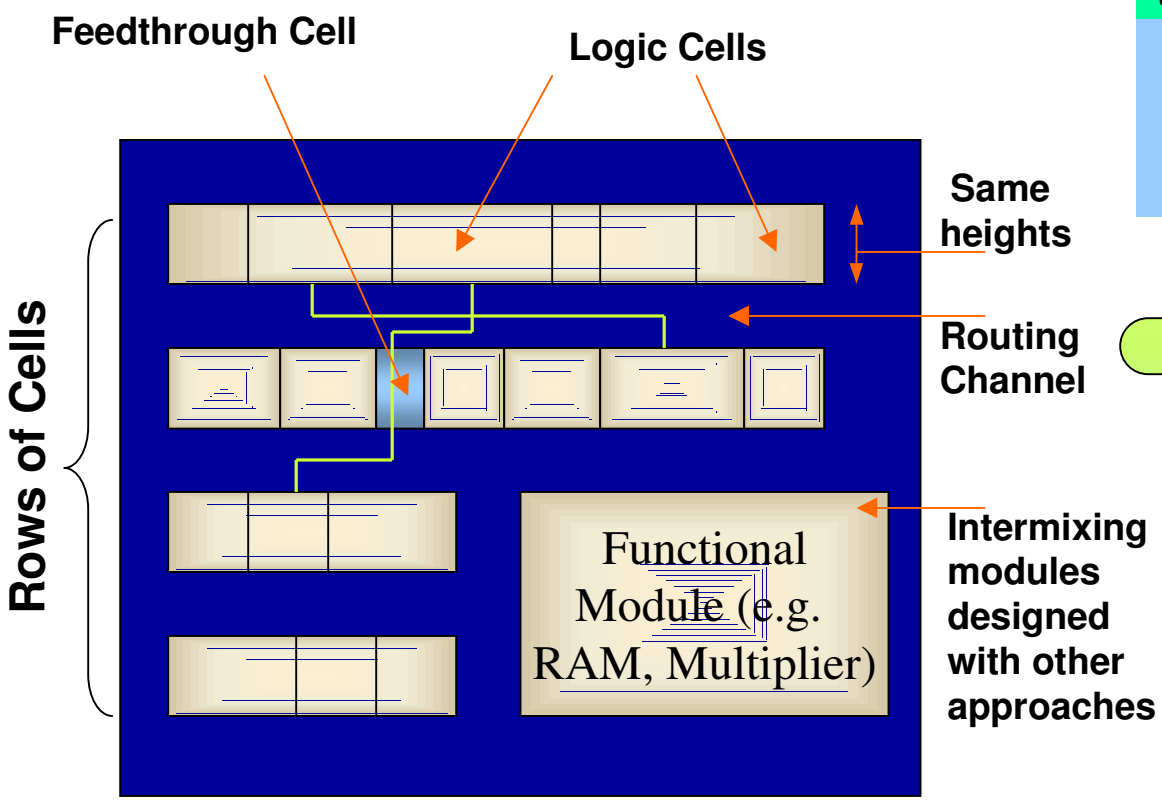
Cell-Based Design (Standard Cell)

Popular Approach

Cells custom designed and verified only once

Reduce implementation effort by reusing limited number of cells in library

What to include in a cell library ???



Some libraries provide large cells to ensure high driving capabilities; this detrimental to area and power

Alternatively, some other libraries provide different versions of each cell, with small, medium, and large driving capacity

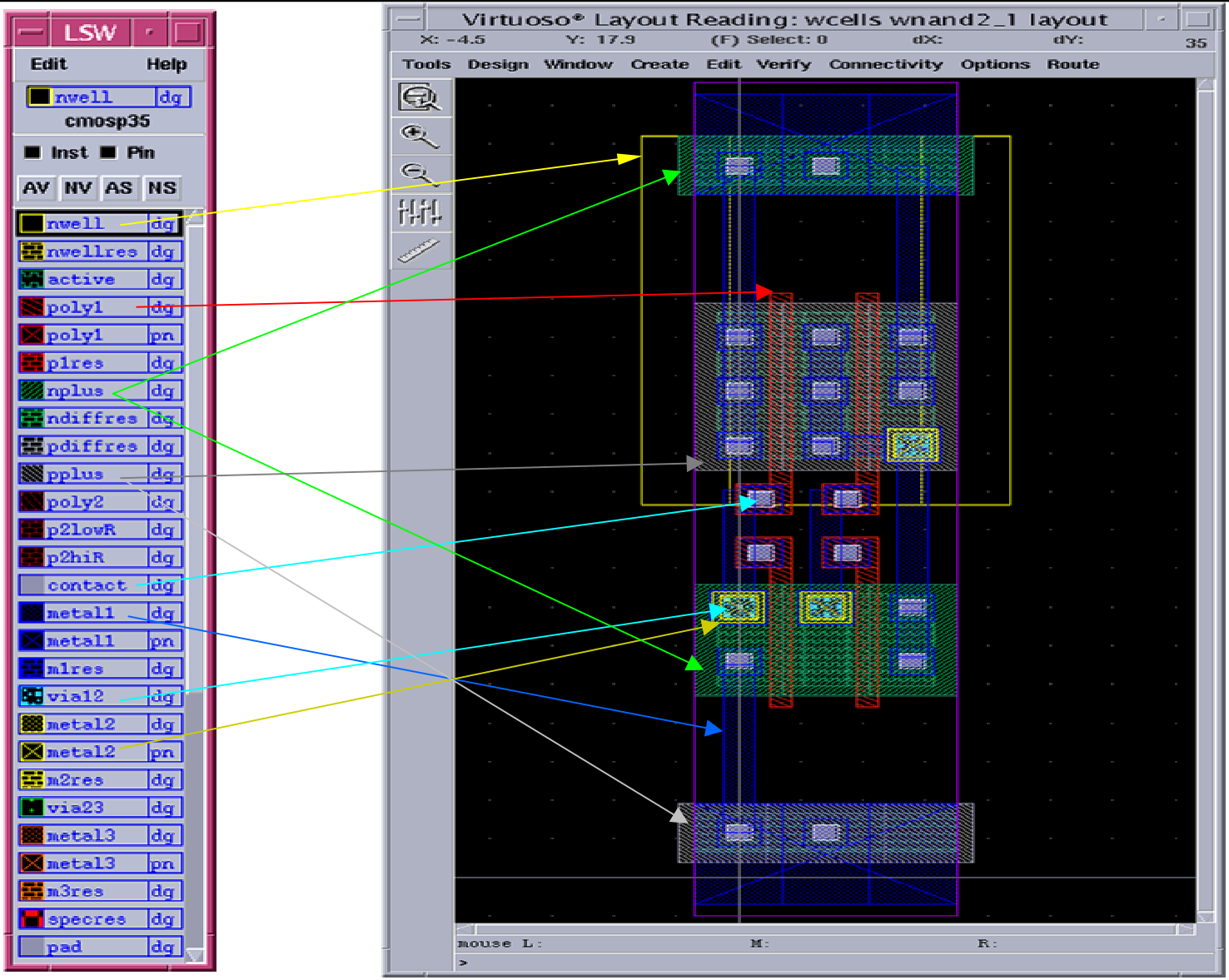
Documentation

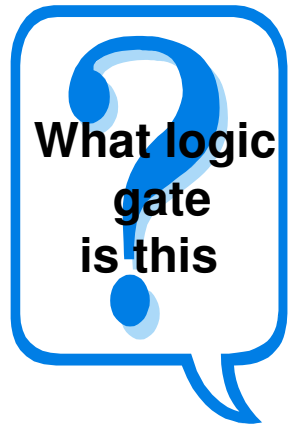
-Function
-Size & terminals
-Delay and power in terms of load capacitance and input rise and fall times

Cell Library

MUX
INV
NOR
NAND
XOR
Counter
Full-Adder
Encoder
Decoder
Comparator

Layout of a Cell-Library CMOS Logic Gate





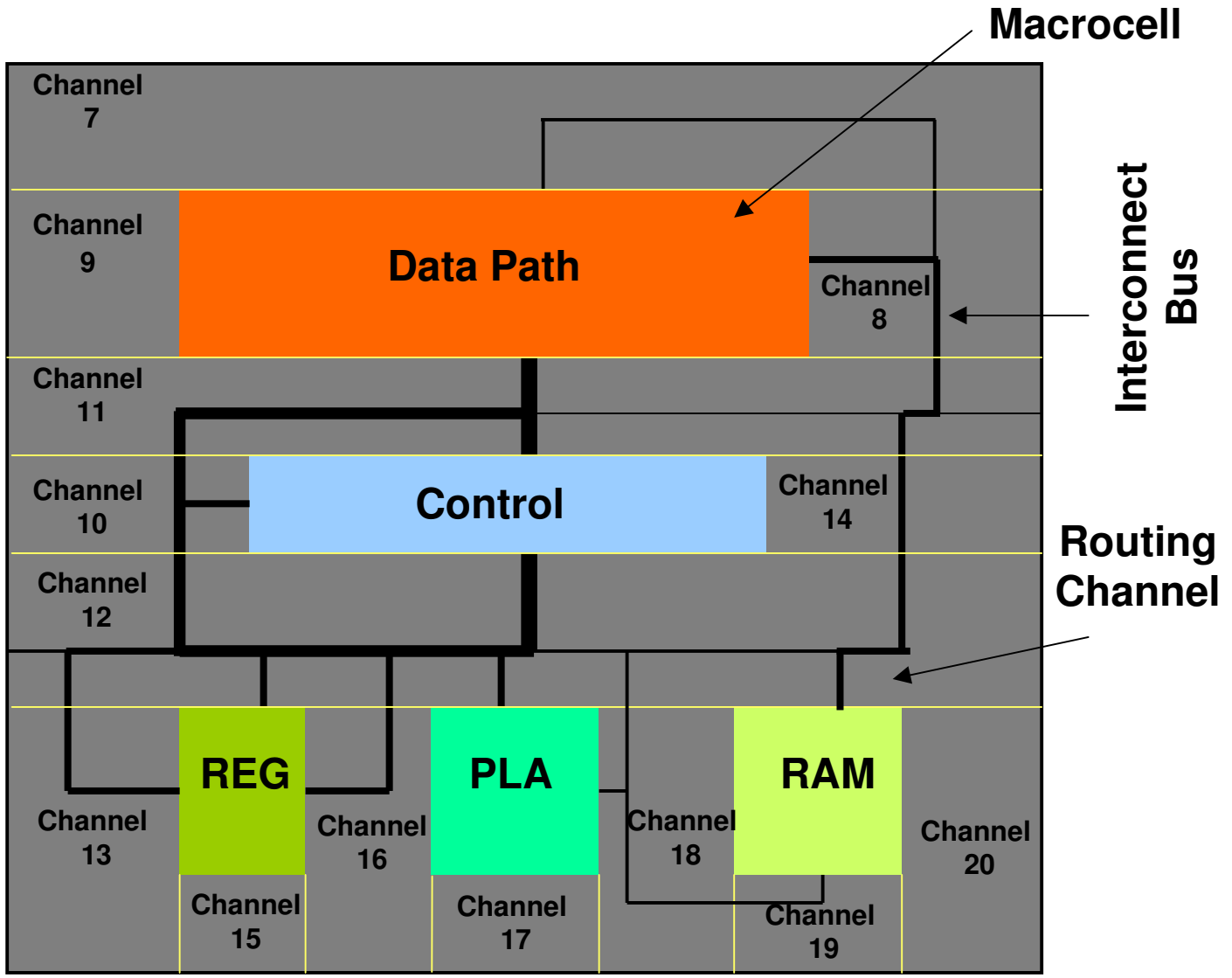
Courtesy of Cadence Design systems

Macrocell Design Methodology

Taking advantage of regular structures like PLAs, memories, adders, and multipliers

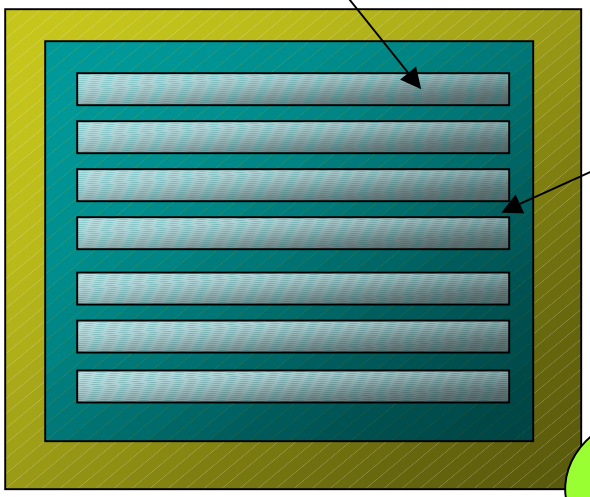
Macrocell generator is parameterizable and produces an optimized layout of a module

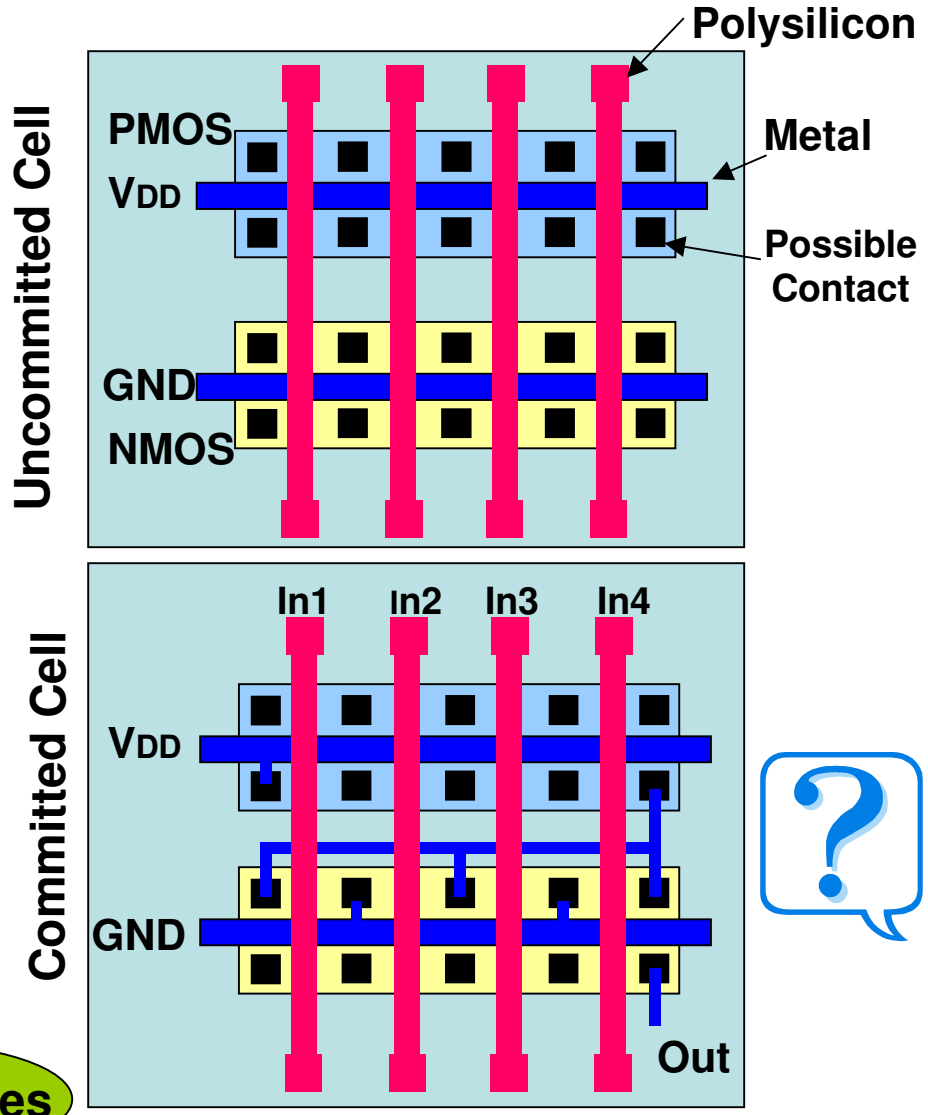
Last step is placement and Routing such chip area is optimized



Masked Gate Arrays

Programmable gate arrays reduce design and manufacturing processing time in expense of lower performance, integration density, and higher power





Gate Arrays

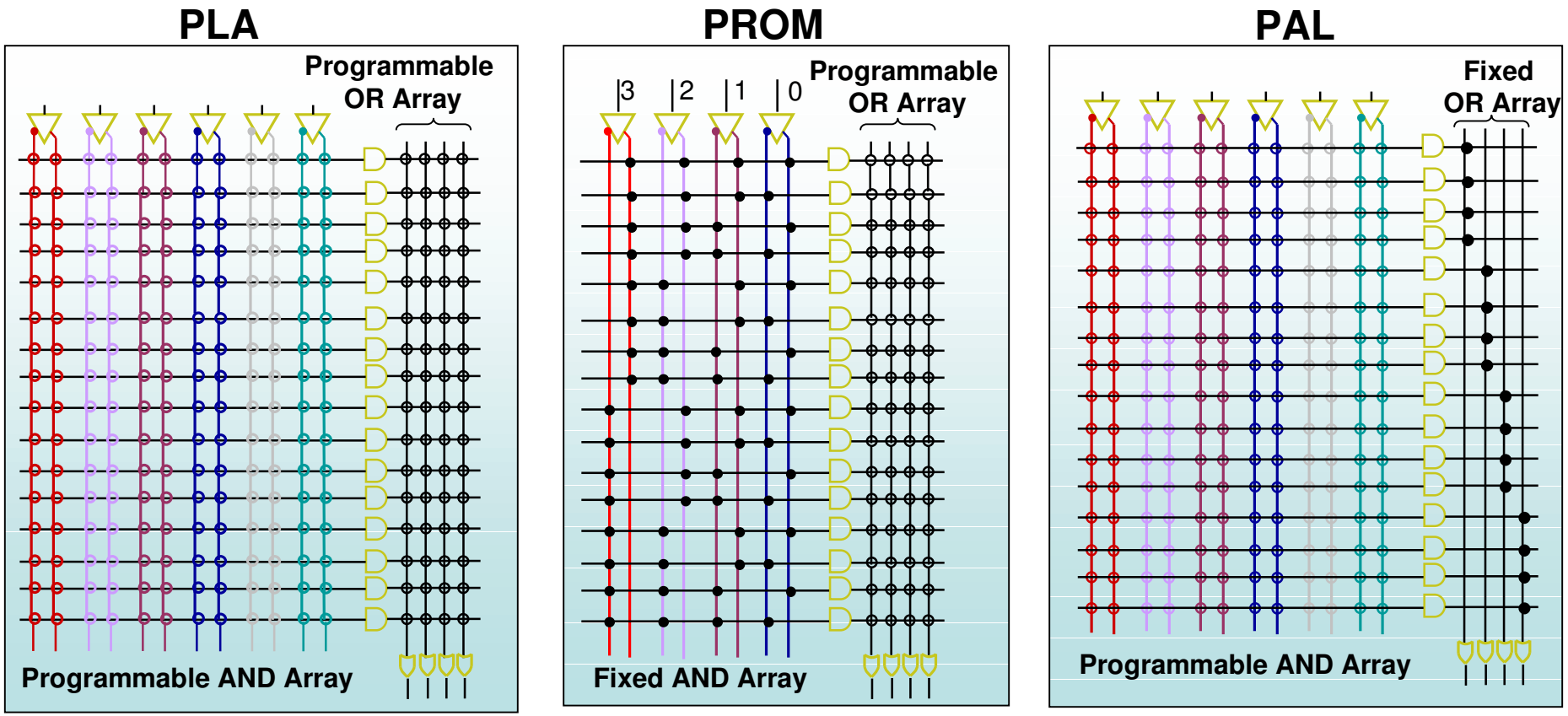
Prediffused wafers that only require metallization steps

Sea-of-Gates

Programmable Logic Devices

Fuse-Based preprocessed die programmed (once only) in field

Prewired arrays with no need for dedicated manufacturing steps



Flexible to implement arbitrary functions in sum-of-product

Trade flexibility for density and performance, compared to PLA

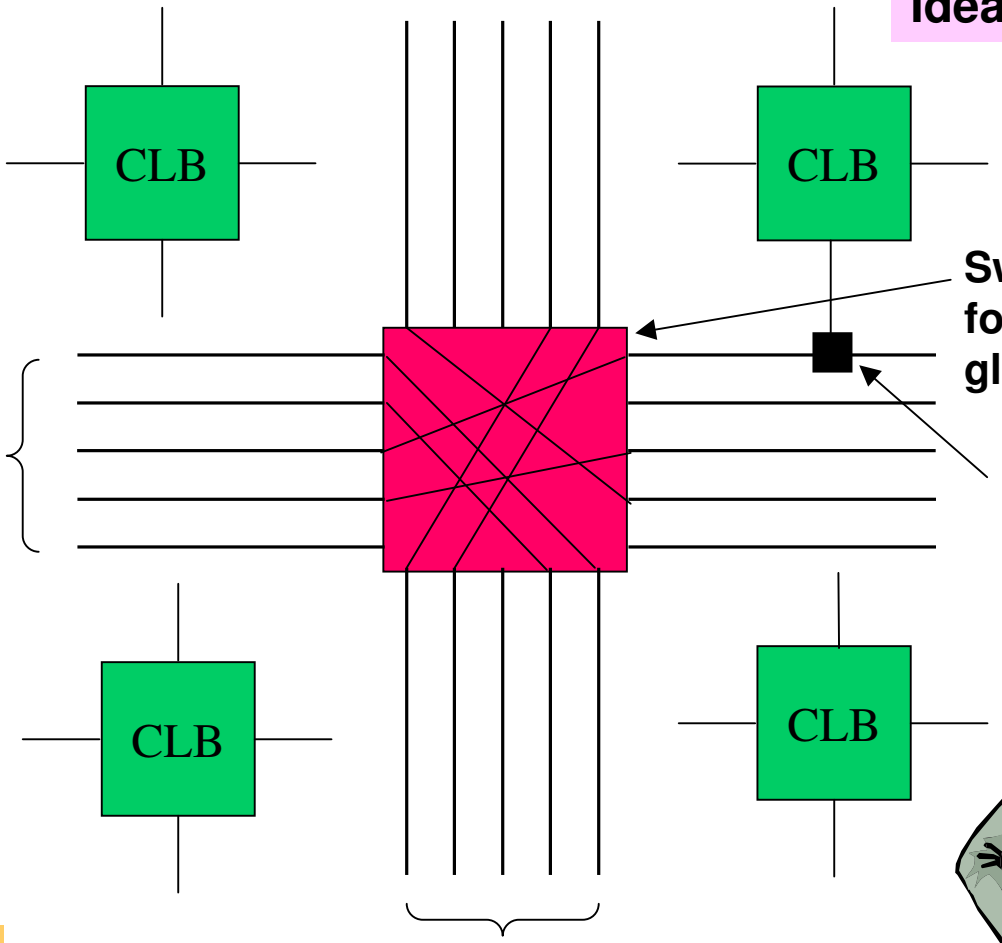
Solid circles indicate fixed connection

Hollow circles indicates programmable connection

Field Programmable Gate Arrays (FPGA)

Repeatable Programming

Ideal for prototyping

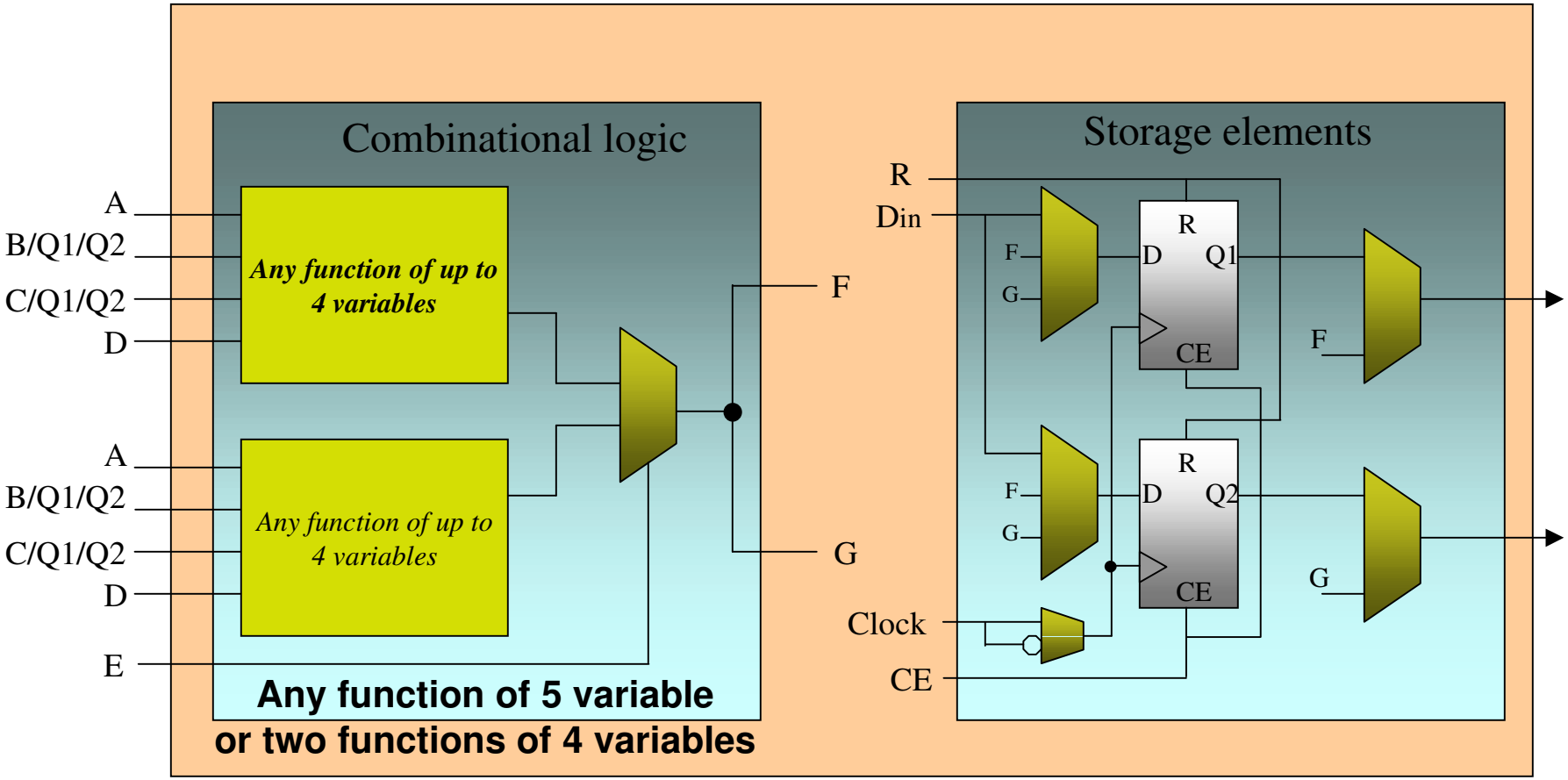


Short Turn-Around Time

Increasingly used in products

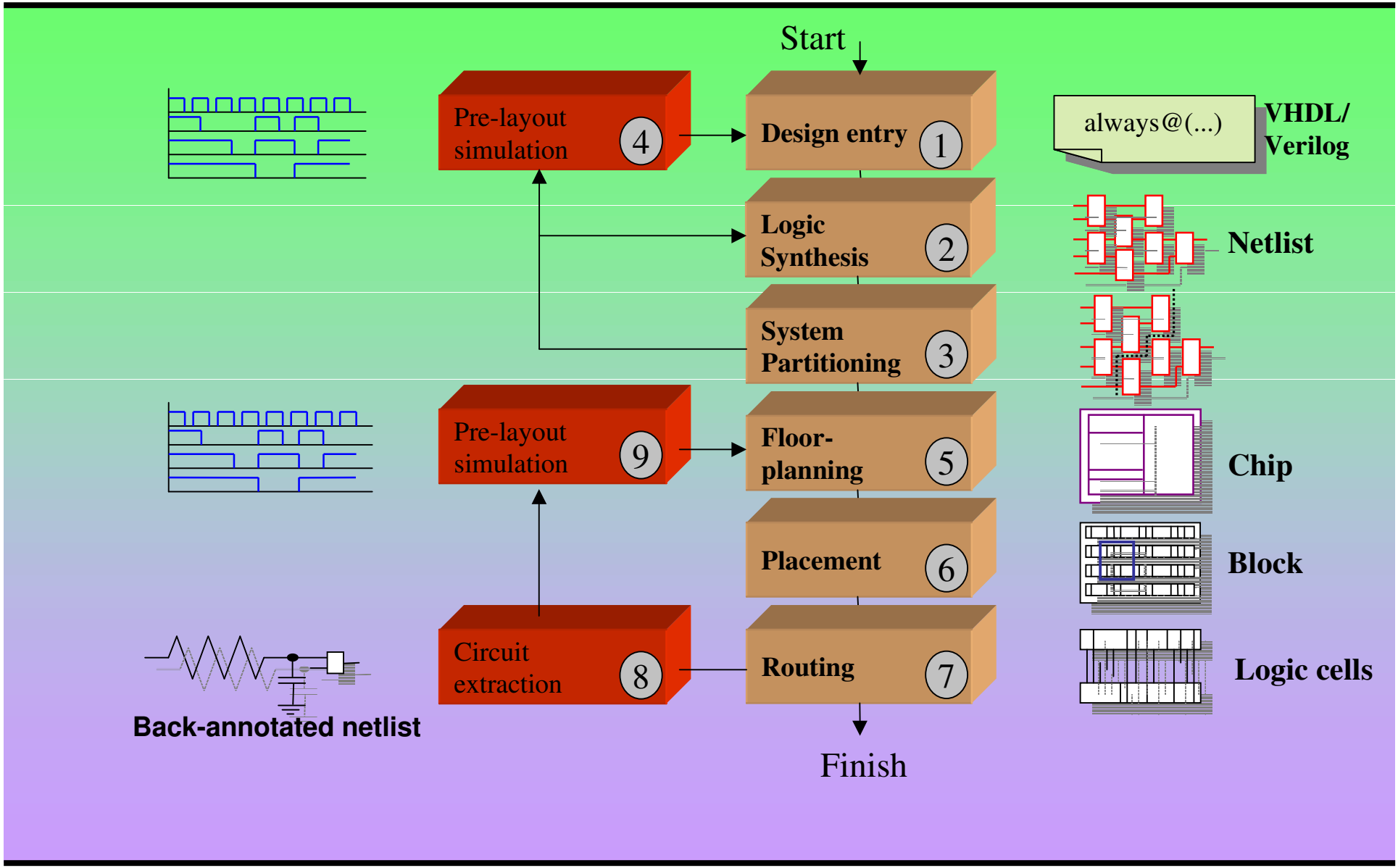
Volatile

Configurable Logic Blocks (CLB)



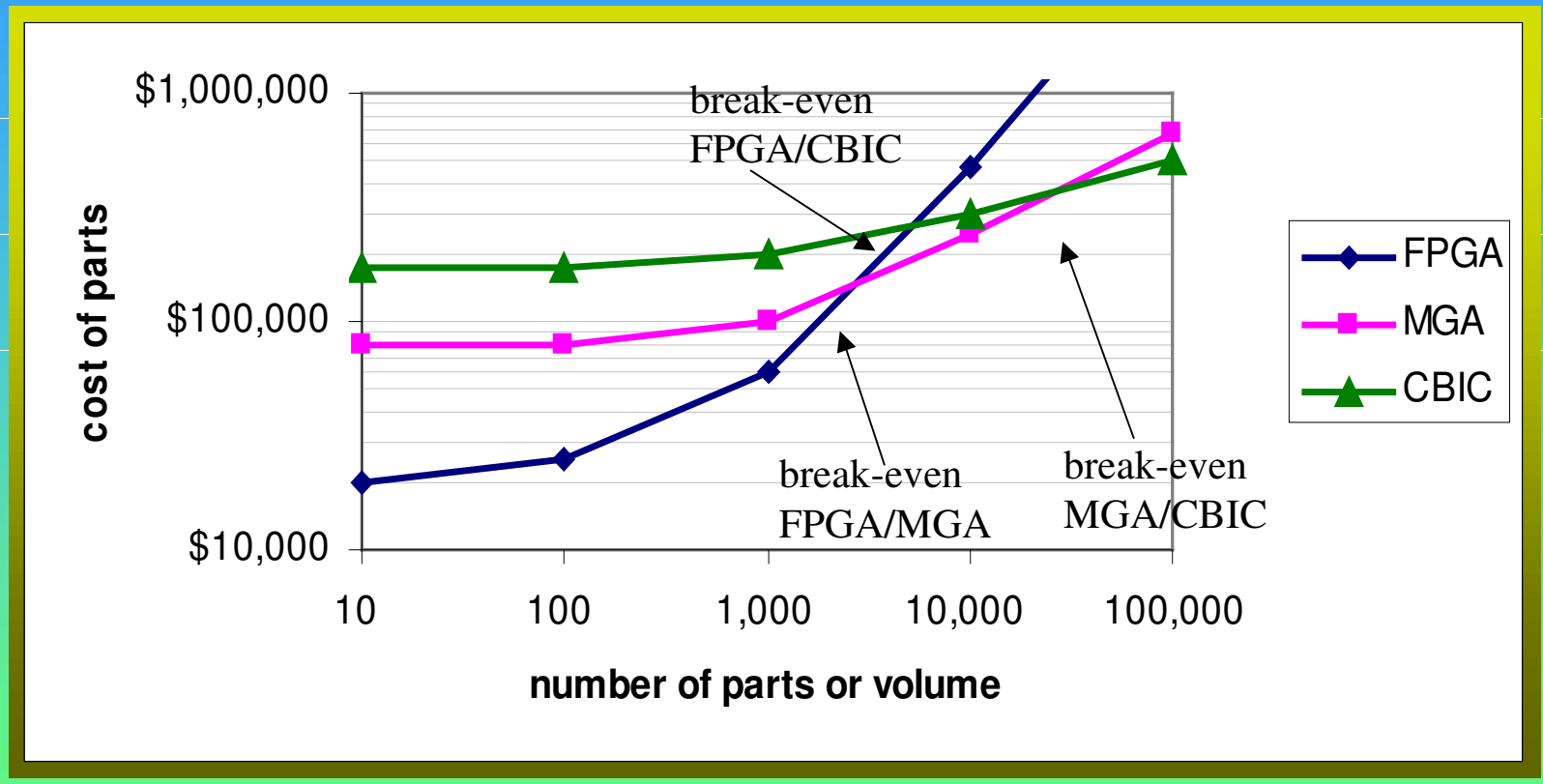
Courtesy of Xilinx

ASIC Design Flow



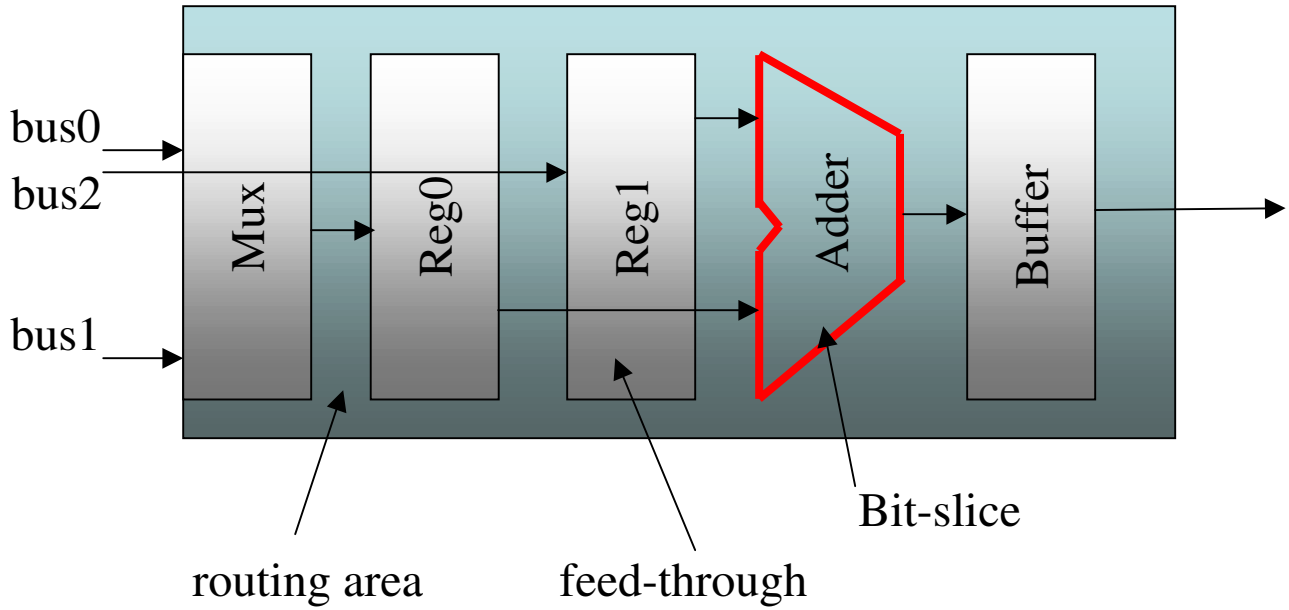
Economics of ASICs

Total part cost = fixed part cost + variable cost per part * volume of parts

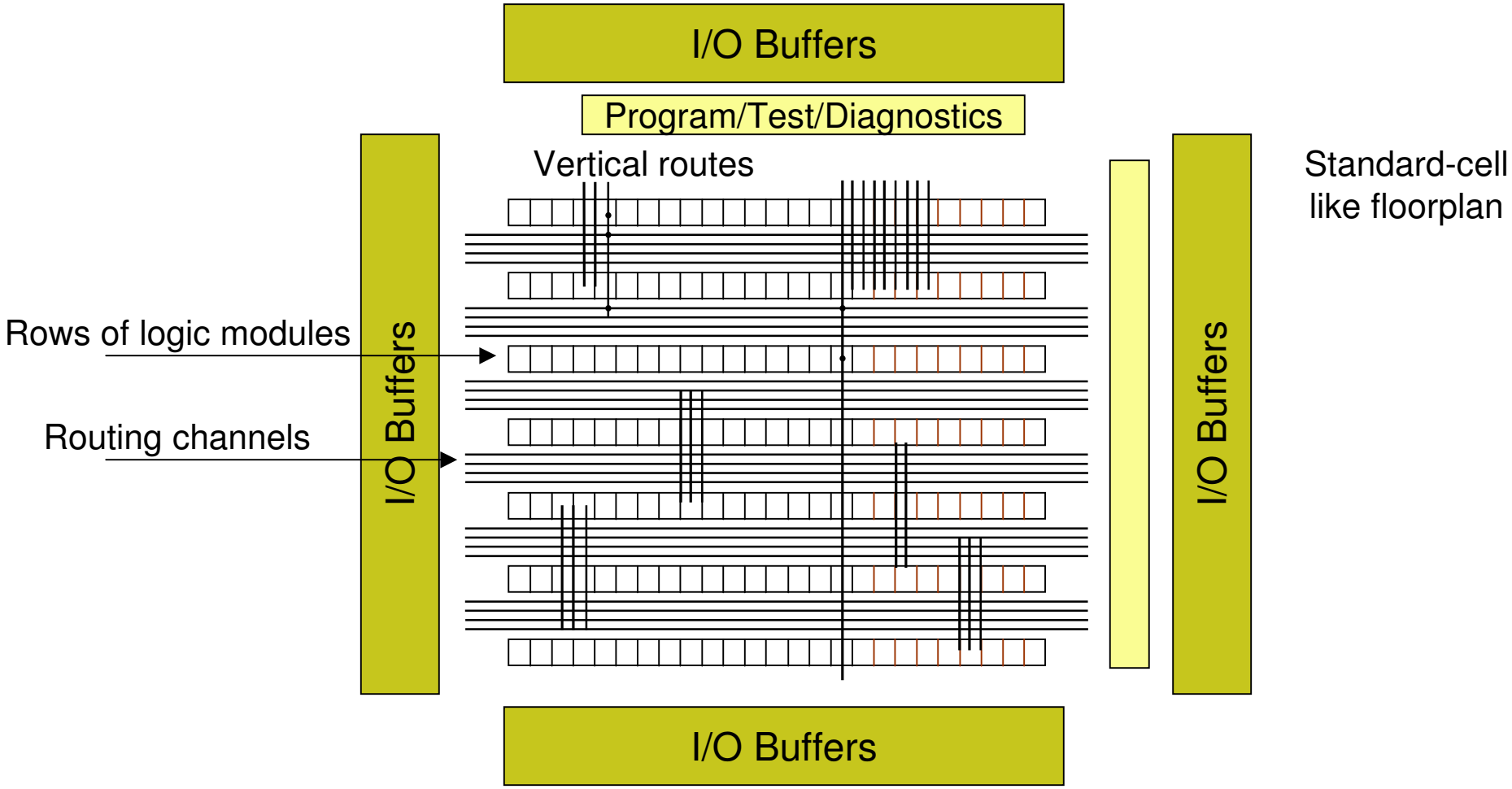


Analysis from "Application-Specific Integrated Circuits" by M. Smith, Addison-Wesley, 1997

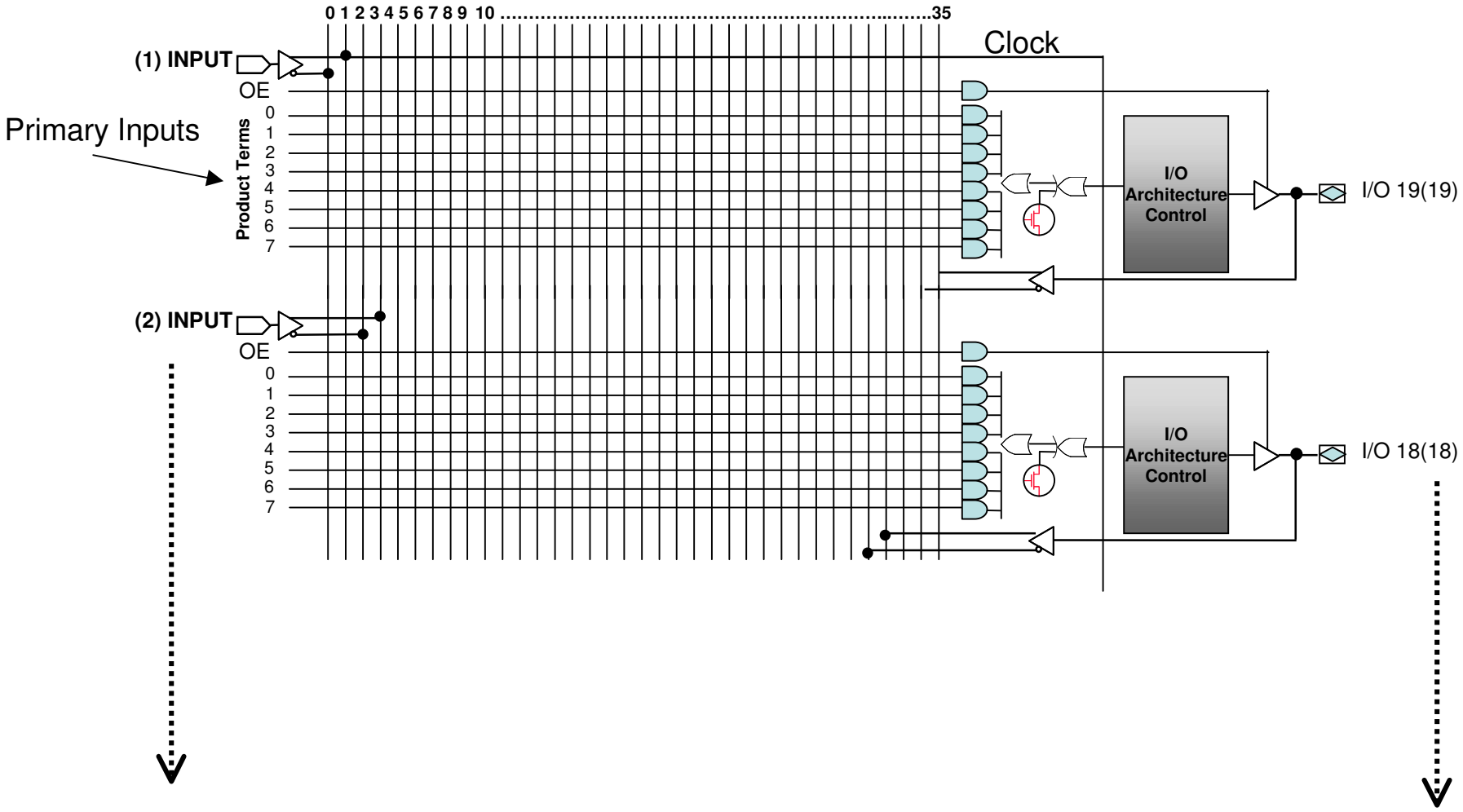
Module Generators Compiled Datapath



Advantages: One-dimensional placement/routing problem



Erasable PLD



Macrocell *Altera Corp*

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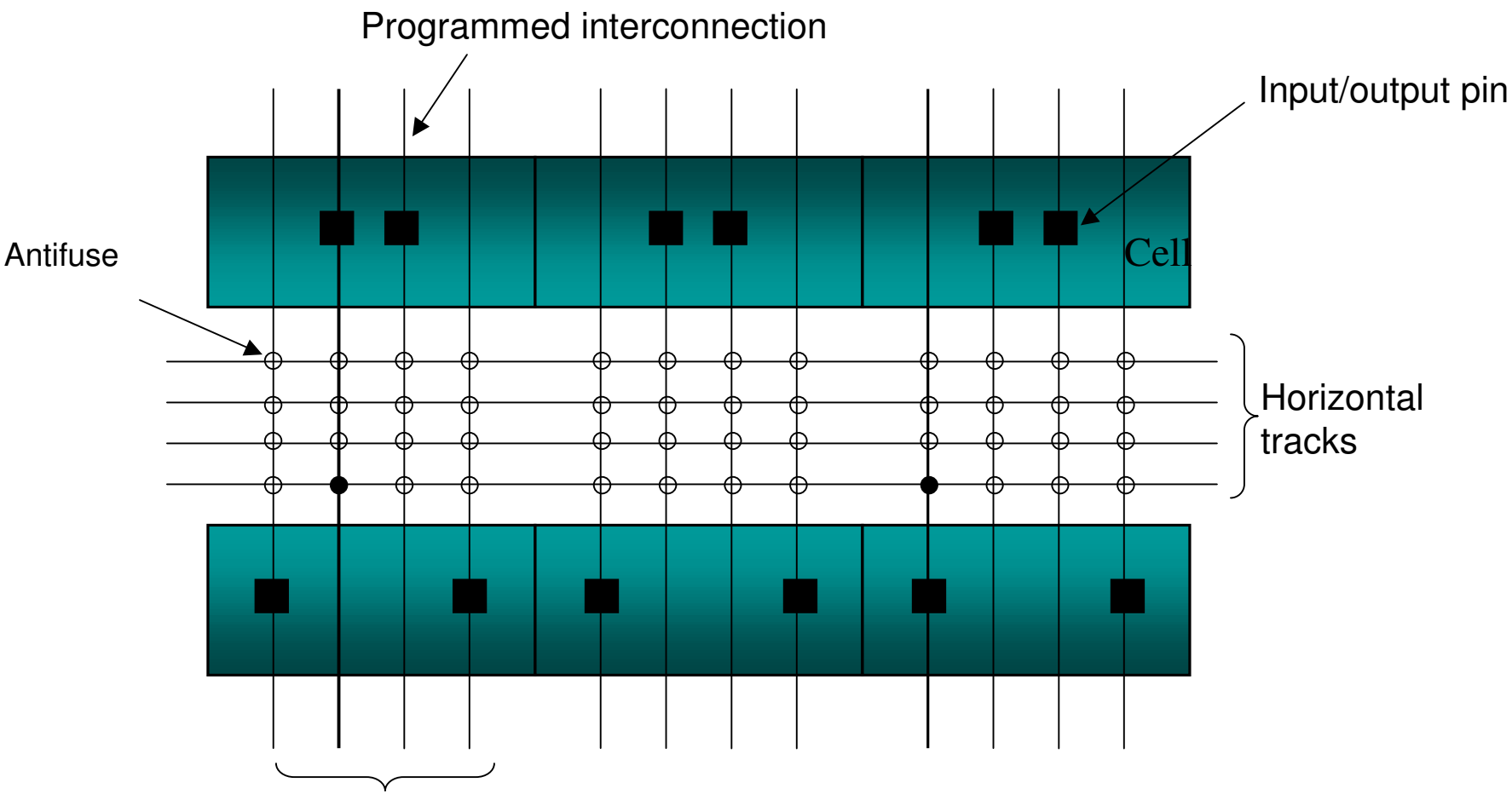
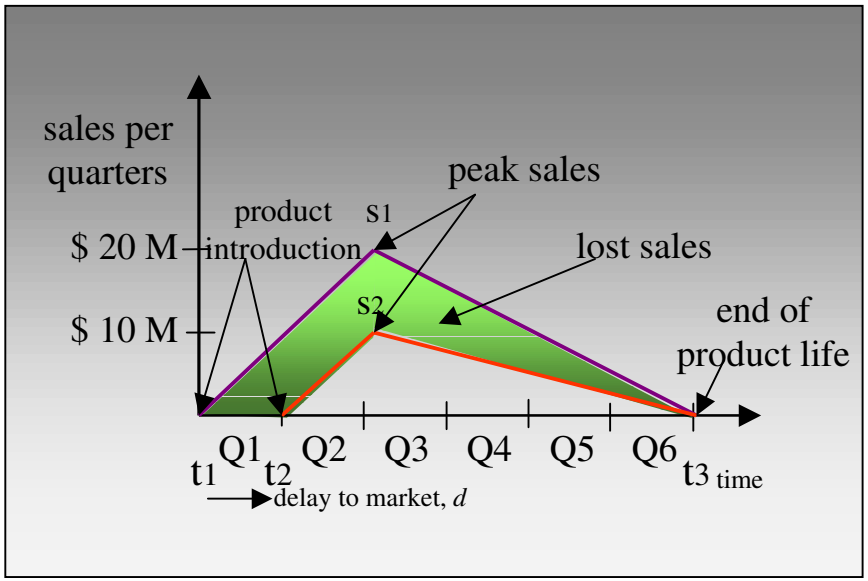
Interconnect



Programming interconnect using anti-fuses

A Profit Model



Price per gate figures