Midterm Exam, Winter 2001, March 2

ELE-350: Digital Electronics

Department of Electronics, Carleton University

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Aids: Calculator ID: _____

Q1	Q2	Q3	Q4	Q5	Total
/20	/15	/15	/25	/25	/100

* Write your name and ID number on all pages. Attempt all questions.

* If you are asked to make an assumption, then you must use it, but only for that particular question.

* You have two hours to write the exam. Approximate timing is given for each question. If you follow that, you should have 15 minutes at the end to review your answers.

Formula

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\phi_0}\right)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_H - V_L)(1-m)}[(\phi_0 - V_H)^{1-m} - (\phi_0 - V_L)^{1-m}]$$

$$V_T = V_{T0} + r(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_{D(sat)} = \frac{k'_n}{2}\frac{W}{L}(V_{Gs} - V_T)^2(1 + \lambda V_{Ds})$$

$$I_{D(lin)} = k'_n \frac{W}{L}\left[(V_{DD} - V_T)V_{DS} - \frac{V^2_{DS}}{2}\right]$$

$$V_M = \frac{r(V_{DD} - |V_{TP}|) + V_{TN}}{1 + r}, \quad r = \sqrt{\frac{k_p}{k_n}}$$

Data

NMOS: L=1.2um, V_{TO}=0.74V, $k' = 19.6\times10^{-6}\,A/V^2$, $\lambda = 0.06\,V^{-1}$, $C_{gdo} = C_{gso}$=0.43fF/um, C_j=0.3fF/um, C_{jsw}=0.8fF/um, t_{ox}=200E-10m.

PMOS: L=1.2um, V_{TO}=0.74V, $k' = 5.4\times10^{-6}\,A/V^2$, $\lambda = 0.19\,V^{-1}$, $C_{gdo} = C_{gso}$=0.43fF/um, C_j=0.5fF/um, C_{jsw}=0.135fF/um, t_{ox}=200E-10m.

General: m=0.5 (abrupt junction), ϕ_0 =0.6V, ε_{ox}=3.5E-13F/cm

[1] (20 marks, 2 marks each) [15 minutes] Briefly explain the following terms and concepts. In each case no more than two sentences are needed to make your point.

1.a) CMOS:
Complementary Metal-Oxide-Semiconductor (Silicon) is an IC fabrication technology that uses both PMOS and NMOS transistors.

1.b) Transistor Threshold Voltage
Minimum voltage applied between the gate and source of a MOS transistor to turn it on, i.e. to make it pass current.

1.c) Logic Gate Switching Threshold Voltage:
Voltage applied ot a logic gate (w.r.t grammd) to make the output switch to the same voltage, i.e, the midpoint of V_{TC} (V_{out}=V_{in}).

1.d) Abstraction in Digital Electronics
To model a design at one level such that its internal details are hidden from the higher level of abstraction.

1.e) Regenerative Property

A basic property of a logic gate which ensure that a distributed signal gradually converges to one of nominal voltage levels after raising through a number of gates.

1.f) Channel Length Modulation
In saturation mode current increases by increasing V_{DS} due to a reduction in effective channel length, which is called channel length modulation.

1.g) General Scaling in IC Technology
Scaling the device dimensions and the voltages by two different factors to ensure effectiveness and feasibility (i.e. being realistic)

1.h) Static Power Dissipation
Power consumed by a circuit when inactive, i.e. while it si not switching.

1.i) Fan-in and fan-out
Fan-in is the number of inputs to a logic gate.
Fan-in is the number of logic gates driven by one.

1.j) Depletion MOSFET
A MOSFET that due to charges implemented under its gate area is normally on (at $V_{GS}=0$). It needs some V_T to be turned off.

[2] (15 marks) [15 minutes] Answer the following questions.

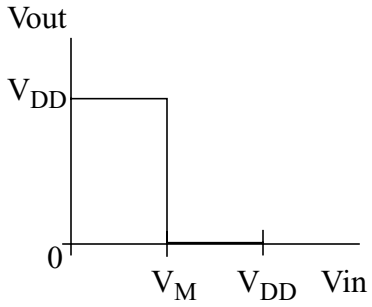
2.a) (6 marks) Plot the VTC of an ideal logic gate and indicate what are its input resistance, output resistance, noise margins high and low, output voltages high and low, switching threshold voltage, and voltage swing?

$R_{in}=\infty$, $R_{out}=0$,

$NM_H=NM_L=V_{DD}/2$, $V_{OH}=V_{DD}$

$V_{OL}=0$, $V_M=V_{DD}/2$,

$V_{swing}=V_{OH}-V_{OL}=V_{DD}$



2.b) (5 marks) What is the significance of Noise Marin? Also express NM_H and NM_L in terms of the output and input high and low voltage. Define each of V_{OH}, V_{OL}, V_{IH}, V_{IL}.

Noise margin shows how noise tolerance a logic gate is.

$NM_L=V_{IL}-V_{OL}$ $NM_H=V_{OH}-V_{IH}$
* V_{IH} is the minimum recognizable “1” input

* V_{IL} is the maximum recognizable “0” input
[at Vin=V_{IH} or Vin=V_{IL} $\partial Vout/\partial Vin$=-1]

V_{OH} and V_{OL} are the nominal output voltage of a logic gate
[such that V_{OH} =f(V_{OL}) and V_{OL} =f(V_{OH})]

2.c) (4 marks) State two reason for keeping the power dissipation down in digital integrated circuits?

To reduce the heat generated and avoid damaging the chip or high cooling costs.
To avoid frequent battery charging in portable and wireless electronics applications.

[3] (15 marks, 5 marks each part) [15 minutes] A CMOS conventional inverter with a load capacitance of 1pF is once operated with a supply voltage of 5V (case 1) and once with a supply of 3V (case 2). Assume no channel length modulation and assume that the transistors operate in saturation for high-to-low an low-to-high output trtansitions to $V_{DD}/2$.

3.a) Which one is faster? By how many percents?

$$\frac{t_{p2}}{t_{p1}} = \frac{\frac{CV_{DD2}}{2I_2}}{\frac{CV_{DD1}}{2I_1}} = \frac{V_{DD2}}{V_{DD1}} \cdot \frac{I_1}{I_2} = \frac{V_{DD2}}{V_{DD1}} \cdot \frac{(V_{DD1}-V_T)^2}{(V_{DD2}-V_T)^2} = \frac{3}{5} \cdot \frac{(5-0.75)^2}{(3-0.75)^2} = 2.13$$

Case 2 is slower by 213%, or speed in case 2 is 1/2.13=47% of case 1.

3.b) Which one is more energy consuming per cycle? By how many percents?

$$\frac{E_2}{E_1} = \frac{CV^2_{DD2}}{CV^2_{DD1}} = \frac{3^2}{5^2} = 0.36$$ Energy consumption in case 2 is 36% of case 1.

3.c) If operated at their own maximum frequency, which inverter case consumes more power? By how many percents?

$$\frac{P_2}{P_1} = \frac{E_2 \cdot f_2}{E_1 \cdot f_1} = \frac{E_2}{E_1} \cdot \frac{t_{p1}}{t_{p2}} = 0.36 \times 0.47 = 0.17$$

Power dissipation in case 2 (at max frequency) is 17% of case 1 (at its max frequency).

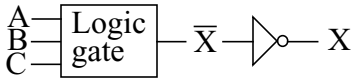
[4] (25 marks) [30 minutes] The carry output of a full-adder can be expressed as X=AB+C(A+B). Implement this function in conventional CMOS. In the circuit, you are allowed to used the primary inputs only, not their inversions.

4.a) (3 marks) Can you implement this function, with the given restriction, in one stage (i.e. one logic gate) only? Explain why.

No. One can not implement a “non-inverted” function in one stage using conventional CMOS. In a conventional CMOS logic gate an inversion always happens, because the PMOS (pull-up) section that gives high output is triggered by low inputs and NMOS section that gives low output is triggered by high inputs.

4.b) (5 marks) Implement X by inspeciton only, using the duality property of the PMOS and NMOS networks in a CMOS logic gate.

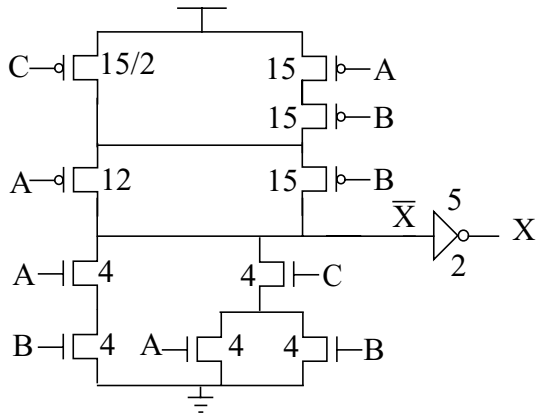
Since we can not implement in one stage.
we do it in two stages, i.e.
we implement $\overline{x}$ and add an inverter.



we do NMOS part first, because we have form

$$\overline{X} = \overline{AB + C(A + B)}$$

Then we do PMOS part by using duality, i.e, series--->parallel, parallel--->series

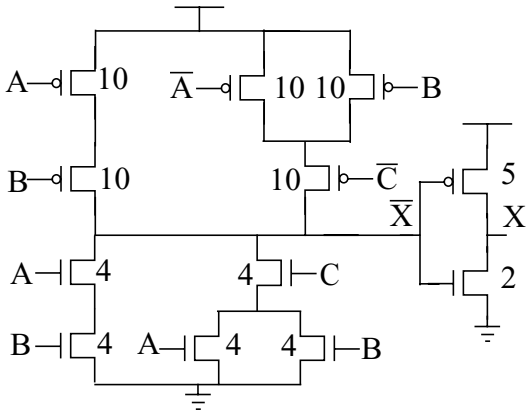


4.c) (5 marks) Now implement X using DeMorgan’s low.

$$\overline{X} = \overline{AB + C(A + B)} = \overline{AB} \cdot \overline{C(A + B)} = (\overline{A} + \overline{B})(\overline{C} + \overline{A}\overline{B})$$

$$\overline{X} = (\overline{A}+\overline{B})\overline{C} + (\overline{A}+\overline{B})\overline{A}\,\overline{B} = (\overline{A}+\overline{B})\overline{C} + \overline{A}\,\overline{A}\,\overline{B} + \overline{B}\,\overline{A}\,\overline{B} = (\overline{A}+\overline{B})\overline{C} + \overline{A}\,\overline{B}$$

4.d) (5marks) Oops.. don't panic, if you do it right you get two different circuits. Size the transistors in both circuits such that, in worst cases, each stage (i.e each logic gate) has the output resistance of an inverter with PMOS W/L=5 and NOMOS W/L=2. Do this on the figures in part (b) and (c)



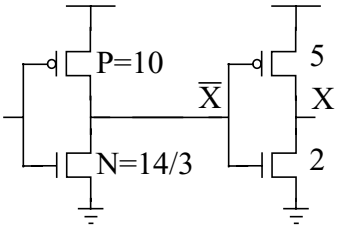
4.e) (2 marks) Which implementation do you prefer? Why?

Prefer C, because it gives lower capacitances at output ($\overline{X}$).

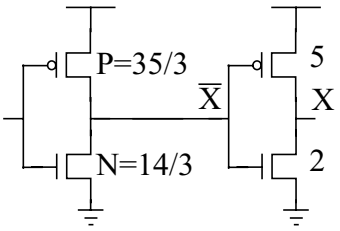
[C has smaller area over all and is faster because of less parasitics]

4.f) (5 marks) What are the equivalent inverter circuits for each implementation (b and c) in the very best cases of rising and falling delay. Draw the equivalent inverter circuits.

b: P=(15+15)||15=10; N=2+(4||8)=14/3



c: P=5+20||10=35/3; N=2+(4||8)=14/3



[5] (25 marks) [30 minutes] Consider a ring oscillator with five CMOS inverters operating with a power supply voltage of VDD=3.3V. ALL PMOS transistors are of size W/L=10 and all NMOS transistors are of size W/L=5. Assume that a source or a drain of a PMOS transistor is a square of sides Wp. Similarly a source or a drain of an NMOS transistor is a square of side Wn. Ignore all gate-drain and gate-source overlap capacitances, i.e. no Miller effect too.

5.a) (15 marks) Calculate the period of oscillation.
5.b) (7 marks) Calculate the power dissipation of the oscillator.
5.c) (3 marks) Calculate the switching threshold of each inverter.

a) Calculate Keq. values first for half swing transistors.

NMOS L-->H: V_{Low} =0, V_{high}=-1.65V

$$Keq = \frac{-0.6^{0.5}}{(-1.65)\times(0.5)}[(0.6+1.65)^{0.5}-(0.6)^{0.5}] = 0.681$$

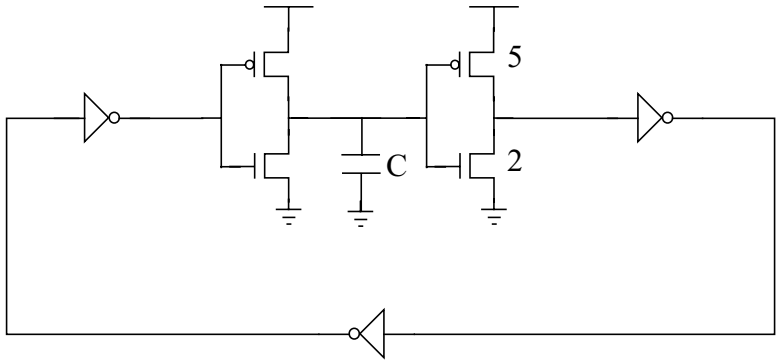
NMOS H-->L: V_{High} =-3.3V, V_{Low}=-1.65V

$$Keq = \frac{-0.6^{0.5}}{(-3.3+1.65)\times(0.5)}[(0.6+3.3)^{0.5}-(0.6+1.65)^{0.5}] = 0.446$$

Values for PMOS are just opposite :

Keq|(NMOS, L-->H)=0.681V, Keq|(NMOS, H-->L)=0.446

Keq|(PMOS, L-->H)=0.446V, Keq|(PMOS, H-->L)=0.681



$AD_P = Wp^2 = (1.2 \times 10)^2 = 144\,um^2$

$PD_p = 2(Wp+Wp) = 2(24) = 48\,um^2$

$AD_n = Wn^2 = (1.2 \times 5)^2 = 36\,um^2$

$PD_n = 2(Wn+Wn) = 2(12) = 24\,um^2$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.5\times10^{-13}}{200\times10^{-10}} = 1.75\,fF/um^2$$

C=Cg|(PMOS, 10)+Cg|(NMOS, 5)+Cd|(PMOS, 10)+Cd|(NMOS, 5)

$$C = Cox(AGp + AGn) + K_{eqp} \times (AD_p C_{jn} + PD_p C_{jsw_p}) + K_{eqn} \times (AD_n C_{jn} + PD_n C_{jsw_n})$$

$AG_P = WpXL = 12X1.2 = 14.4\,um^2$

$AG_n = WnXL = 6X1.2 = 7.2\,um^2$

$C_{L-->H}$=1.75X14.4+1.75X7.2+0.446(144X0.5+48X0.135)+0.681(36X0.3+24X0.8)=93fF

$C_{H-->L}$=1.75X14.4+1.75X7.2+0.681(144X0.5+48X0.135)+0.446(36X0.3+24X0.8)=105fF

--- Calculation I_{ave} Values

$I_{L-->H}$ PMOS:

$$I_{sat} = \frac{k'_p}{2}\frac{W}{L}(V_{DD}-V_T)^2(1+\lambda V_{DD}) = \frac{5.4\times10^{-6}}{2}\times10(3.3-0.74)^2(1+0.19\times3.3) = 0.29mA$$

$$I_{lin} = k'_p\frac{W}{L}\left[(V_{DD}-V_T)\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right] = 5.4\times10^{-6}\times10\left[(3.3-0.74)\frac{3.3}{2}-\frac{3.3^2}{8}\right] = 0.15mA$$

$I_{H-->L}$ NMOS:

$$I_{sat} = \frac{k'_n}{2}\frac{W}{L}(V_{DD}-V_T)^2(1+\lambda V_{DD}) = \frac{19.6\times10^{-6}}{2}\times5(3.3-0.74)^2(1+0.06\times3.3) = 0.38mA$$

$$I_{lin} = k'_n\frac{W}{L}\left[(V_{DD}-V_T)\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right] = 19.6\times10^{-6}\times5\left[(3.3-0.74)\frac{3.3}{2}-\frac{3.3^2}{8}\right] = 0.28mA$$

I_{ave}(L-->H)=(0.29+0.15)/2=0.22mA

I_{ave}(H-->L)=(0.38+0.28)/2=0.33mA

$$t = \frac{CV_{DD}}{2I} \quad t_{PLH} = \frac{93\times3.3}{2\times0.22} = 698pS \quad t_{PHL} = \frac{105\times3.3}{2\times0.33} = 525pS$$

$$t_P = \frac{t_{PLH}+t_{PHL}}{2} = 611.5pS$$

$$T = 2\times t_P\times N = 2\times611.5\times5 = 6115pS = 6.1nS$$

b)

$P = C_L V_{DD}^2 f$ per node

Need to recalculate Keq for full swing. This will be average of already calculated Keqs

Keq=(0.681+0.446)/2=0.564

$C_L = 1.75 \times 14.4 + 1.75 \times 7.2 + 0.564(144 \times 0.5 + 48 \times 0.135) + (0.564)(36 \times 0.3 + 24 \times 0.8)$

=99fF

Total Power=$C_L V_{DD}^2 f \cdot N = 99 \times 3.3^2 \times \frac{1}{6.1} \times 5 = 0.88 mW$

c)

$V_M = \frac{r(V_{DD} - |V_{TP}|) + V_{TN}}{1 + r}, \; r = \sqrt{\frac{k_p}{k_n}}$

$r = \sqrt{\frac{k'_p \left(\frac{W}{L}\right)_p}{k'_n \left(\frac{W}{L}\right)_n}} = \sqrt{\frac{5.4 \times 10}{19.6 \times 5}} = 0.75$

$V_M = \frac{0.75(3.3 - 0.74) + 0.74}{1 + 0.75} = 1.52 V$