Assignment 2

ELE-350: Digital Electronics

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1. Implement the equation X=((A+B)(C+D+E)+F)G using conventional CMOS technique.

a. Verify your implementation using Demorgan's theorem. [1]

b. You realize hat there are more than one way of arranging the transistors for this same fucnition. Suggest as topology (i.e. arrangement or configuration) that gives you the lowest delay and a topology that gives you the highest delay. Explain why in each case. [2]

c. Size the devices such that the output resistance is the same as that of a inverter with NMOS W/L=1 and PMOS W/L=3.

a)

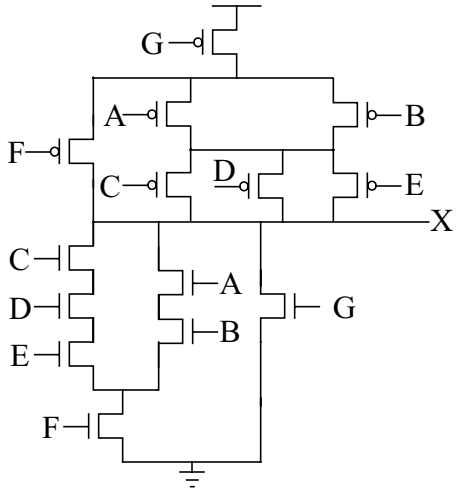
$$\overline{X} = \overline{((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\overline{G}}$$

$$= \overline{((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})} + G$$

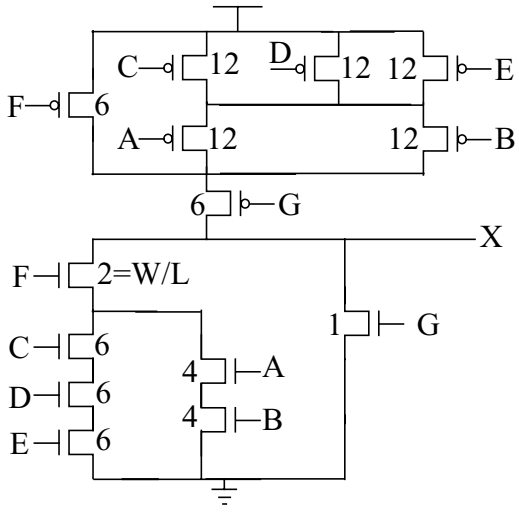
$$= \overline{((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E})} \cdot F) + G$$

$$= (\overline{\overline{A} + \overline{B}} + \overline{\overline{C} + \overline{D} + \overline{E}}) \cdot F + G$$

$$= ((AB + CDE) \cdot F) + G$$



b) Topology (a) gives highest delay because it has highest parasitic capacitance at output. The following topology gives lowest delay, because it only has one PMOS and two NMOS diffusion capacitances at output.



c) In (b) transistors are sized such that any NMOS path has $(W/L)_{eff}=1$ and any PMOS path has $(W/L)_{eff}=3$.

2. Assume that the logic gate of Problem 1 with the "lowest delay" topology is connected ot an inverter of size NMOS W/L=1 and PMOS W/L=3. The following data are given.

NMOS transistor data: L=1.2 um, $V_{TO} = 0.74V$, $k' = 19.6\times10^{-6}$ A/V^2, $\lambda = 0.06V^{-1}$, $C_{gdo} = 0.43$ fF/um, $C_j = 0.3$ fF/um, $C_{jsw} = 0.8$ fF/um, $t_{ox} = 200$ E-10m, and from layout assume: AD=10um^2, PD=15um, AS=10um^2, PS=15um.

PMOS transistor data: L=1.2um, $V_{TO} = -0.74V$, $k' = 5.4\times10^{-6}$ A/V^2, $\lambda = 0.19V^{-1}$, $C_{gdo} = 0.43$ fF/um, $C_j = 0.5$ fF/um, $C_{jsw} = 0.135$ fF/um, $t_{ox} = 200$ E-10m, and from layout assume: AD=30um^2, PD=40um, AS=30um^2, PS=40um.

General data: $V_{DD} = 3V$, all m=0.5 (abrupt junction), $\phi_0 = 0.6V$, $\varepsilon_{ox} = 3.5$ E-13 F/cm.

a) Calculate the falling, rising, and average delays from the input of the logic gate to the input of the inverter. Ignore all internal node capacitances and assume that the relevant transistors operate in saturation during transition to $V_{DD}/2$. Use the average current formula.

b) Repeat (a) using the RC delay formula. Are the answers close to those of part (a)?
c) Calculate the dynamic energy dissipation per cycle. Again ignore the internal capacitances.

Let's first calculate different K_{eq} values.

H ↑ L

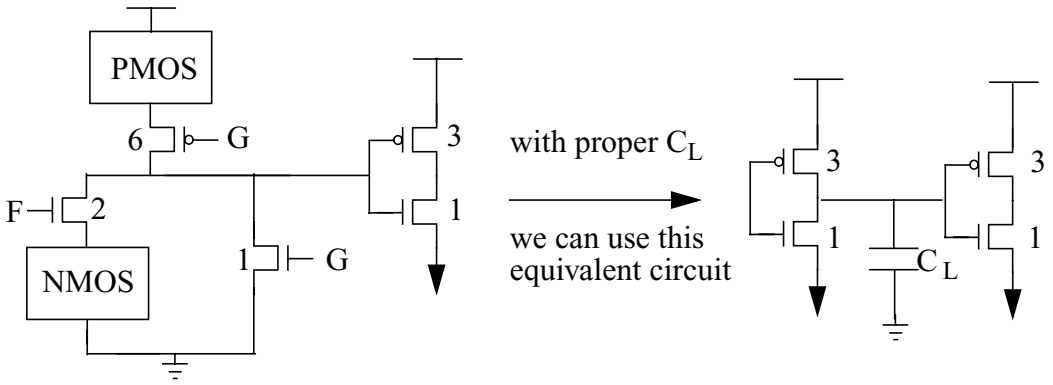
	V_{High}	V_{Low}	K_{eq}
NMOS	-1.5	0	0.697
PMOS	-3	-1.5	0.463

H ↓ L

	V_{High}	V_{Low}	K_{eq}
NMOS	-3	-1.5	0.463
PMOS	-1.5	0	0.697

Note That K_{eq} for $(L\text{--->}H)_{NMOS} = (H\text{--->}L)_{PMOS}$ and $(H\text{--->}L)_{NMOS} = (L\text{--->}H)_{PMOS}$. So , calculating only two values are enough.

a) The schematic is as follows, where only transistors connected to output are shown, because the problem says ignore internal nodes.



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 1.75 \text{ fF/u}m^2.$$

For H--->L

$C_L=C_{db}|_{(PMOS, W/L=6)}+C_{db}|_{(NMOS W/L=1, W/L=2)}+C_g|_{(NMOS W/L=1,PMOS W/L=3)}$

$$C_L = K_{eqp} \times (AD_p C_{jn} + PD_p C_{jsw_p}) + K_{eqn} \times (AD_n C_{jn} + PD_n C_{jsw_n}) + Cox(L \times L + L \times 3L)$$

$$C_L = 14.2 + 2 \times 6.95 + 12.6 = 40.70\,fF$$

For L--->H

$CL=Cdb|_{(PMOS\ 6)}+Cdb|_{(NMOS\ 1,\ 2)}+Cg|_{(NMOS\ 1,\ PMOS\ 3)}=9.44+(2)10.46+12.6=42.96$ fF

Assuming saturation:

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{gs} - V_T)^2(1 + \lambda V_{DS})$$

For H--->L

$I_{NMOS}(V_{out}=3V)=\frac{1}{2}(19.6\times10^{-6})(1)(3-0.74)^2(1+0.06\times3) = 0.059mA$

$I_{NMOS}(V_{out}=1.5V)=\frac{1}{2}(19.6\times10^{-6})(1)(3-0.74)^2(1+0.06\times1.5) = 0.055mA$

I_{NMOS}(ave)=0.057mA

For L--->H

$I_{PMOS}(V_{out}=0V)= \frac{1}{2}(5.4\times10^{-6})(3)(3-0.74)^2(1+0.19\times3) = 0.064mA$

$I_{PMOS}(V_{out}=1.5V)=\frac{1}{2}(5.4\times10^{-6})(3)(3-0.74)^2(1+0.19\times1.5) = 0.055mA$

I_{PMOS}(ave)=0.059mA

$t_{phl} = \frac{3\times40.7}{2\times0.057} = 1.071ns$, $t_{plh} = \frac{3\times42.96}{2\times0.057} = 1.092ns$, $\tau_p = \frac{t_{phl}+t_{plh}}{2} = 1.082ns$

b)

$\tau = 0.69RC_L$

For H--->L $R=1/2(\left.\frac{V_{DS}}{I}\right|_{(NMOS,\ Vout=3V)}+\left.\frac{V_{DS}}{I}\right|_{(NMOS,\ Vout=1.5V)})=1/2(\frac{3}{0.059}+\frac{1.5}{0.055})$=39k

$t_{phl} = 0.69\times39\times40.70 = 1.095ns$

For L--->H

$R=1/2(\left.\frac{V_{DS}}{I}\right|_{(PMOS,Vout=0V)}+\left.\frac{V_{DS}}{I}\right|_{(PMOS,\ Vout=1.5V)})=1/2(\frac{3}{0.064}+\frac{1.5}{0.053})$=37.6k

$t_{plh} = 0.69\times37.6\times42.96 = 1.114ns$

$\tau_p = \frac{1.095+1.114}{2} = 1.1045ns$ values are very close!

c) For energy and power calculations, we must calculate C at output when charged from 0-->V_{DD}. Therefore, a different Keq should be used. No miller effect too.
$Keq|_{(VHigh=-3V,\ VLOW=0V)}=0.58V$.
(Note that this is average of the two Keq. calculated previously!)

$C=Cdb|_{(NMOS\ 1,2)}+Cdb|_{(PMOS\ 6)}+Cg|_{(PMOS\ 3)}+Cg|_{(NMOS\ 1)}=2x8.70+11.82+12.6=41.82\ fF$

$$E = CV_{DD}^2 = 41.82(3)^2 = 0.376\,pJ \quad \text{every/cycle}$$