

Assignment 1

ELE-350: Digital Electronics

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1. Given the data in the following table for an NMOS transistor with $k' = 20 \frac{\mu A}{V^2}$, calculate V_{T0} , λ , Υ , $2|\phi_f|$, and W/L. Use long-channel transistor models.¹

	V_{GS} (V)	V_{DS} (V)	V_{BS} (V)	I_D (μA)
1	3	5	0	1210
2	5	5	0	4410
3	5	10	0	5292
4	5	5	-2	3265
5	5	5	-5	2381

--In all five cases the device is in saturation, i.e. $V_{DS} > V_{GS} - V_T$

--From cases 1 and 2 : $\frac{I_{D2}}{I_{D1}} = \frac{(V_{GS2} - V_{T0})^2}{(V_{GS1} - V_{T0})^2}$, $V_{DS1} = V_{DS2}$ & $V_{BS} = 0$

$$\therefore V_{T0} = \frac{V_{GS2} \cdot \sqrt{\frac{I_{D1}}{I_{D2}}} - V_{GS1}}{\sqrt{\frac{I_{D1}}{I_{D2}}} - 1} = 0.8V$$

--From cases 2 and 3: $\frac{I_{D3}}{I_{D2}} = \frac{(1 + \lambda \cdot V_{DS3})}{(1 + \lambda \cdot V_{DS2})}$, $V_{GS2} = V_{GS3}$

$$\therefore \lambda = \frac{\frac{I_{D2}}{I_{D3}} - 1}{V_{DS2} - \left(V_{DS3} \cdot \frac{I_{D2}}{I_{D3}} \right)} = 0.05 V^{-1}$$

--From $\frac{W}{L} = \frac{2 \cdot I_{D1}}{k'(V_{GS1} - V_{T0})^2(1 + \lambda \cdot V_{DS1})}$, we get $\frac{W}{L} = 20$

--Solve for V_T :

$$V_T = V_{GS} - \sqrt{\frac{2I_D}{K(1 + \lambda \cdot V_{DS})I_{D2}}} \quad \text{where } k = k' \frac{W}{L} = 400 \frac{\mu A}{V^2}$$

$$V_{T4} = 5 - \sqrt{\frac{2 \cdot 3265}{400(1 + 0.05 \cdot 5)}} = 1.386V \text{ for case 4.}$$

$$V_{T5} = 1.914V \text{ like wise for case 5.}$$

On the other hand we can write

$$V_{T4} = V_{T0} - \Upsilon(\sqrt{|-2\phi_F + V_{SB4}|} - \sqrt{|-2\phi_F|})$$

$$V_{T5} = V_{T0} - \Upsilon(\sqrt{|-2\phi_F + V_{SB5}|} - \sqrt{|-2\phi_F|})$$

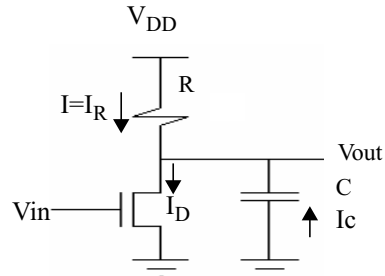
Now you have two equations and two unknowns.

Solve to get $\Upsilon = 0.7V^{0.5}$ and $2|\phi_F| = 0.6V$

¹ Answer: $V_{T0} = 0.8V$, $\lambda = 0.05V^{-1}$, $\Upsilon = 0.7V^{0.5}$, $2|\phi_F| = 0.6V$ and $W/L=20$.

2. For the following NMOS inverter circuit, assume $V_{DD} = 5V$, $R = 75k\Omega$, $W/L=3.6/1.2$, and $C=3pF$. Use the following data for an NMOS transistor: $k' = 19 \times 10^{-6} \frac{\mu A}{V^2}$, $V_{TO} = 0.743V$, and $\lambda = 0.06V^{-1}$, see the answer. ^{2 3 4 5}

- Discuss qualitatively why this circuit behaves as an inverter.
- Find V_{OH} and V_{OL} .
- Calculate t_{plh} (falling delay D_f), t_{phl} (rising delay D_r), and t_p (average delay D).
- Are the rising and falling delays equal? Why?
- Calculate the static power dissipation for: (i) $V_{in}=0V$ and (ii) $V_{in}=5V$.
- Calculate the dynamic power dissipation assuming that the gate is clocked as fast as possible.



- It works as an inverter because
 if $V_{in} < V_T$ (i.e. low), NMOS is off, $I=0 \implies V_{out}=5V$ i.e. High.
 if V_{in} is high (i.e. 5V), NMOS is on, $I \neq 0 \implies V_{out}=5-IR$ i.e. Low.

- For $V_{in} < V_T \implies V_{OH} = 5V$.

For $V_{in} = V_{OH} = 5V$, NMOS is in linear (or triode) mode.

$$I = K_n V_{OL} \left(5 - V_T - \frac{V_{OL}}{2} \right) = \frac{5 - V_{OL}}{R} = I_R = I_D \implies V_{OL} = 0.26V$$

c)

$$-- t_{plh} = 0.64RC = 155ns$$

-- For t_{phl} we should calculate I_{ave}

$$I_C = I_D - I_R$$

$$V_{out} = 5V, I_{D,sat} = 923\mu A, I_R = 0, \implies I_C = 923\mu A$$

$$V_{out} = 2.5V, I_{D,lin} = 589\mu A, I_R = 33\mu A, \implies I_C = 556\mu A$$

$$\implies I_{ave} = I_{c,ave} = 740\mu A; C=3PF$$

Since C is large, we ignore parasitics.

$$t_{phl} = \frac{2.5 \times C}{I_{ave}} = 10.1ns \quad \text{and} \quad t_p = 82.5ns$$

d) $t_{plh} \gg t_{phl}$ because $R = 75K\Omega$ is much larger than the effective on-resistance of NMOS.

e) If $V_{in} = V_{OL} \implies V_{out} = V_{OH} = 5V, I_{VDD} = 0 \implies P_s = 0$

$$\text{If } V_{in} = V_{OH} \implies V_{out} = V_{OL}, I_{VDD} = 63.2\mu A \implies P_s = 0.316mW$$

f) $f_{max} = \frac{1}{t_p} = \frac{12.1}{2}MHz, V_{swing} = V_{OH} - V_{OL} = (5 - 0.26)V$

$$P_d = C \cdot V_{swing} \cdot V_{DD} \cdot f_{max} = (3PF) \cdot (5 - 0.26) \cdot 5 \cdot \left(\frac{12.1}{2}M\right)$$

$$P_d = 0.43mW$$

² Answer (b): $V_{OH}=5V$ and $V_{OL}=0.26V$.

³ Answer (c): $t_{plh}=155ns, t_{phl}=10.1ns$ and $t_p=82.5ns$.

⁴ Answer (e): 0 and 0.316mW.

⁵ Answer (f): $P_d=0.43mW$.