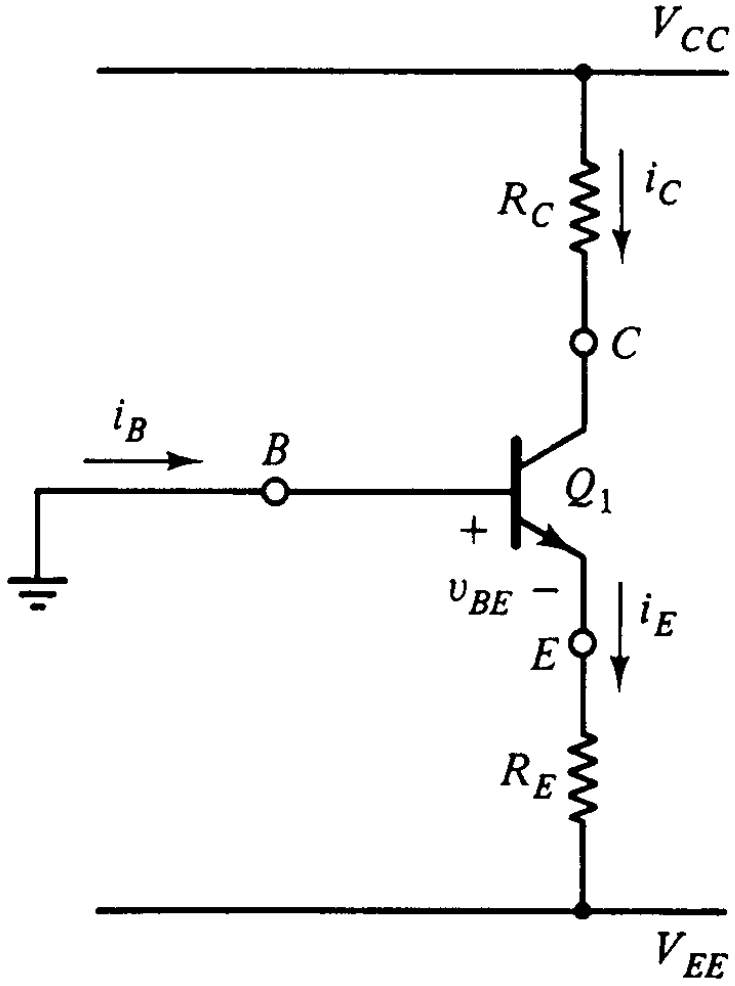
Current Source Biasing

- Integrated circuits have transistors which are manufactured simultaneously with the same device parameters (parameters from chip to chip will vary)
- As a result, different bias techniques are employed than in discrete designs
- One common technique is current source biasing, which allows the designer to take advantage of matched devices
- We will begin by looking at some simple current source circuits
- A current source is not a “naturally” occurring device. It can be simulated by a network of transistors and circuit elements.

Figure 7.31
NPN BJT with grounded base.



The voltage across R_E is approximately constant.

$\therefore$ I_E is held at a constant value

$$I_E = \frac{-V_{EE} - V_{BE}}{R_E}$$

Figure 7.32
Network of R_E and V_{EE} replaced by constant dc current source of equivalent value $I_o = -(V_{EE} - V_{BE})/R_E$.

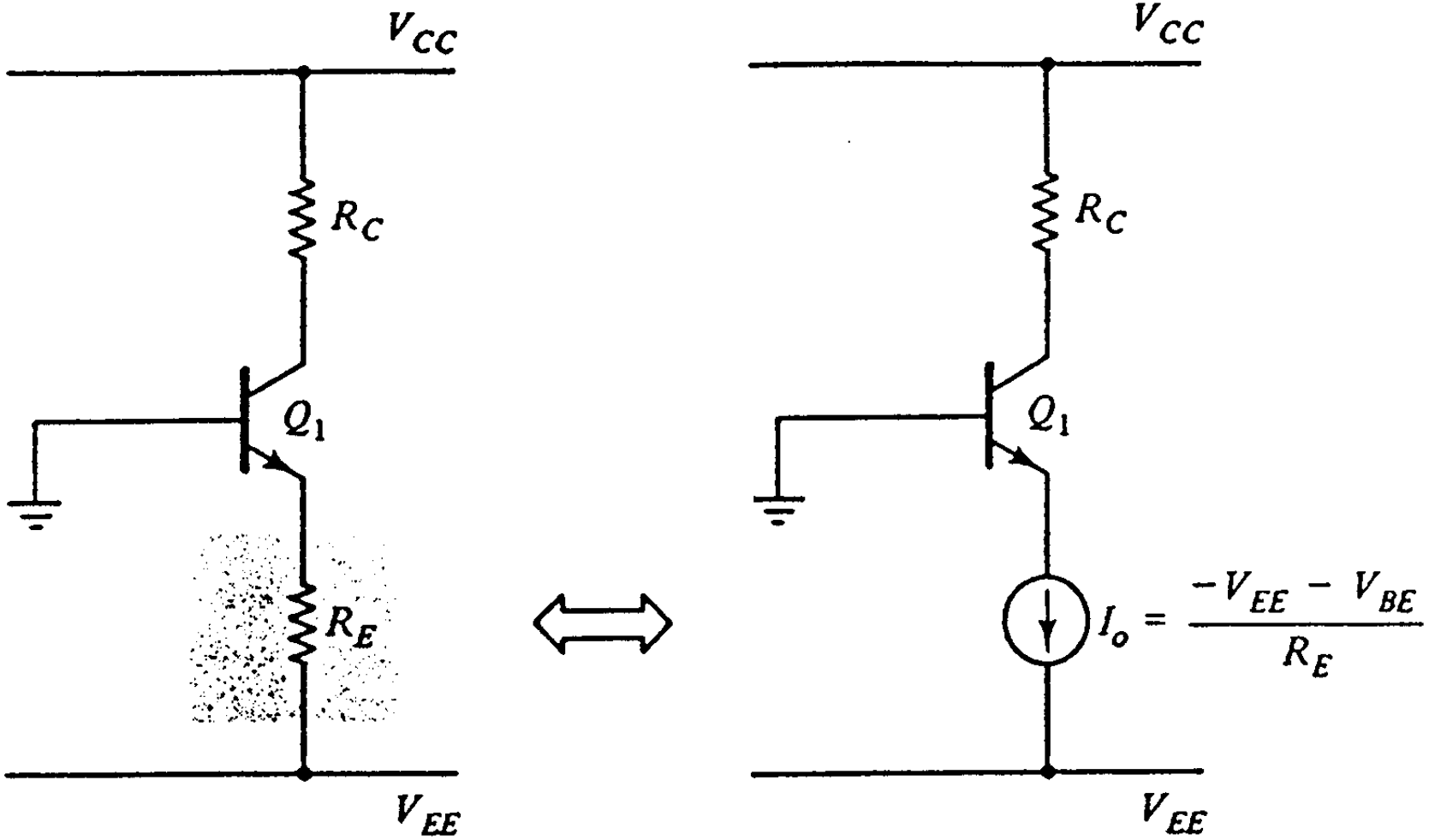


Figure 7.33
Simulated current source using an NPN BJT.

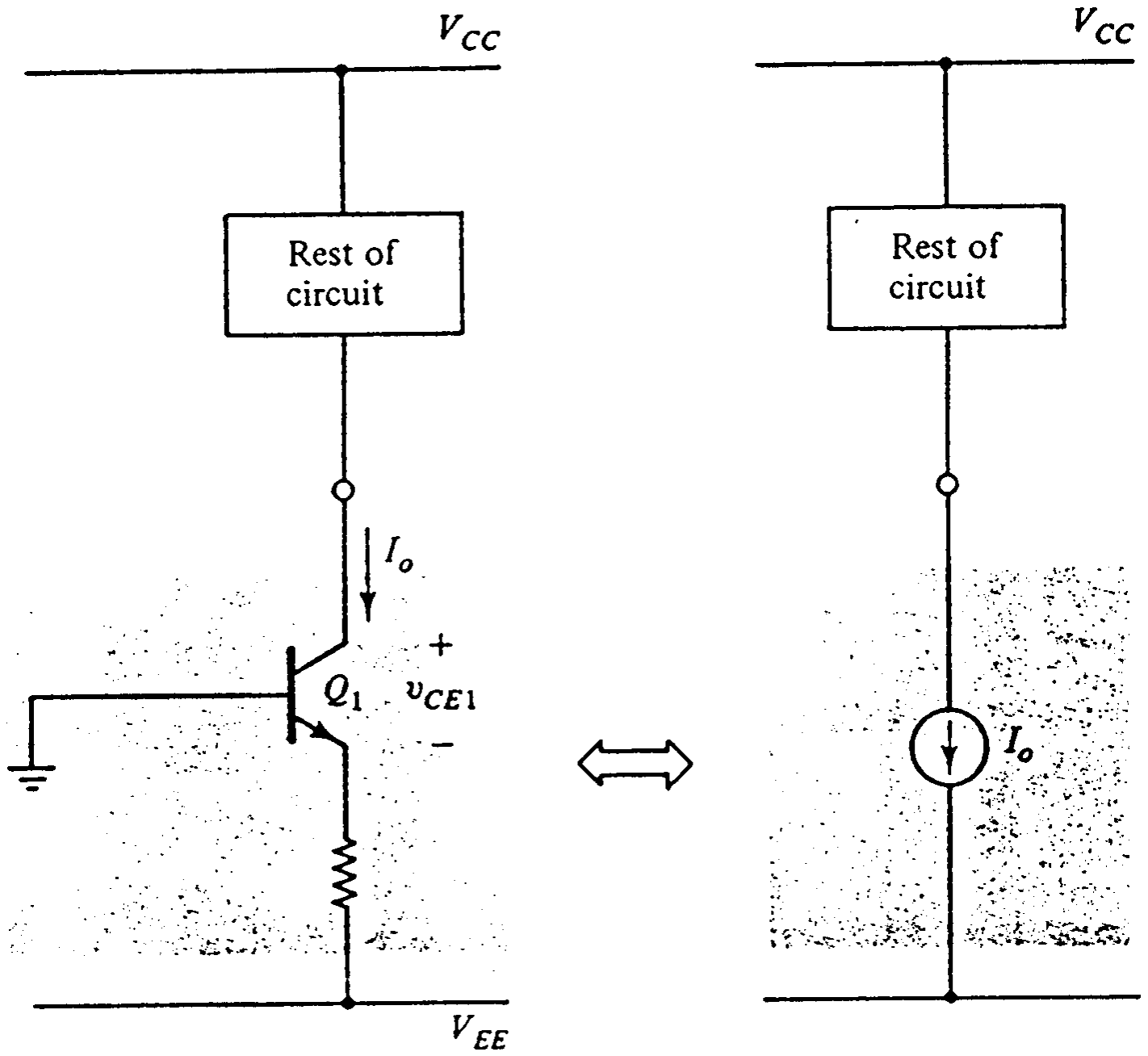


Figure 7.34
BJT follower with BJT current source bias.

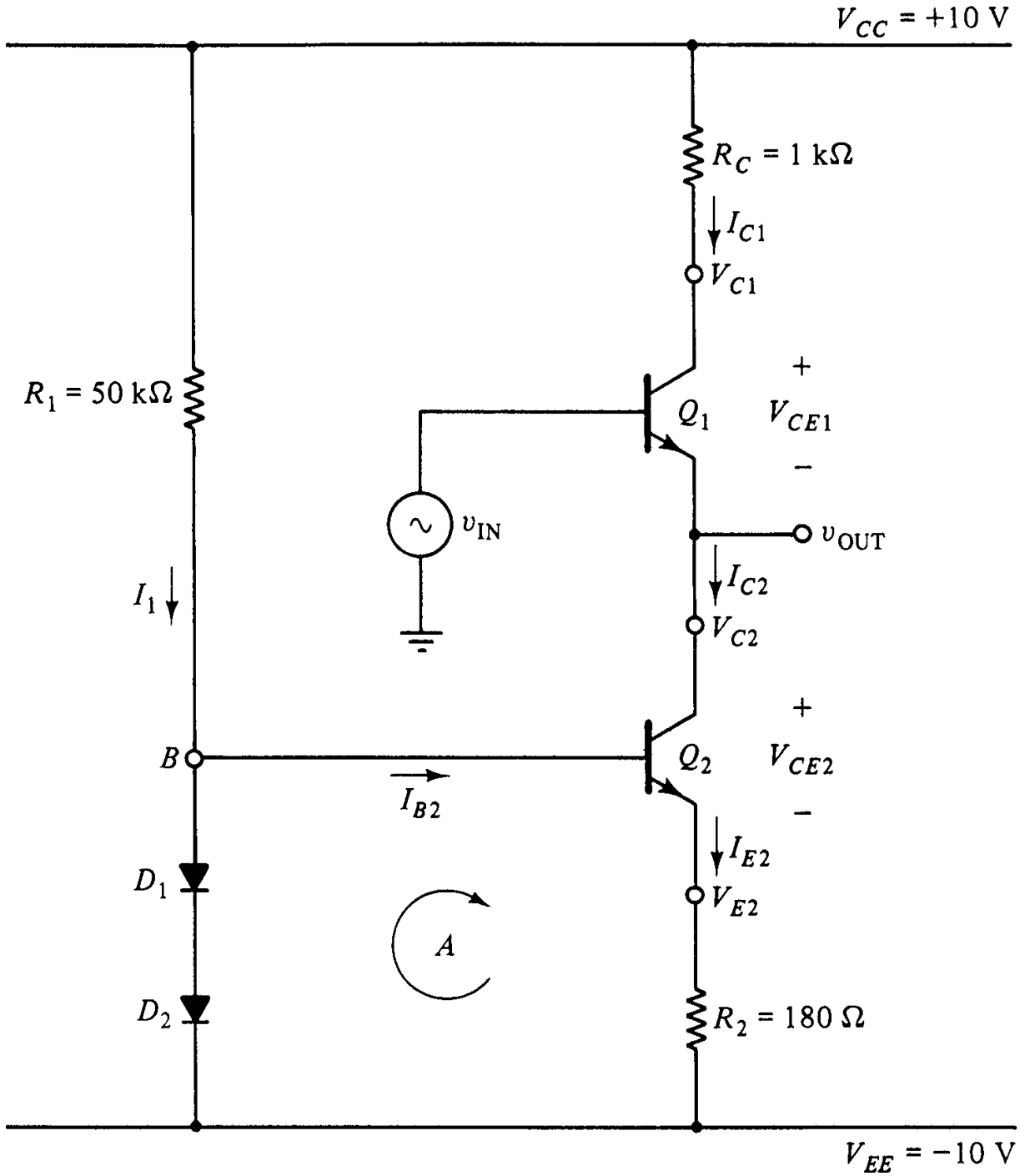
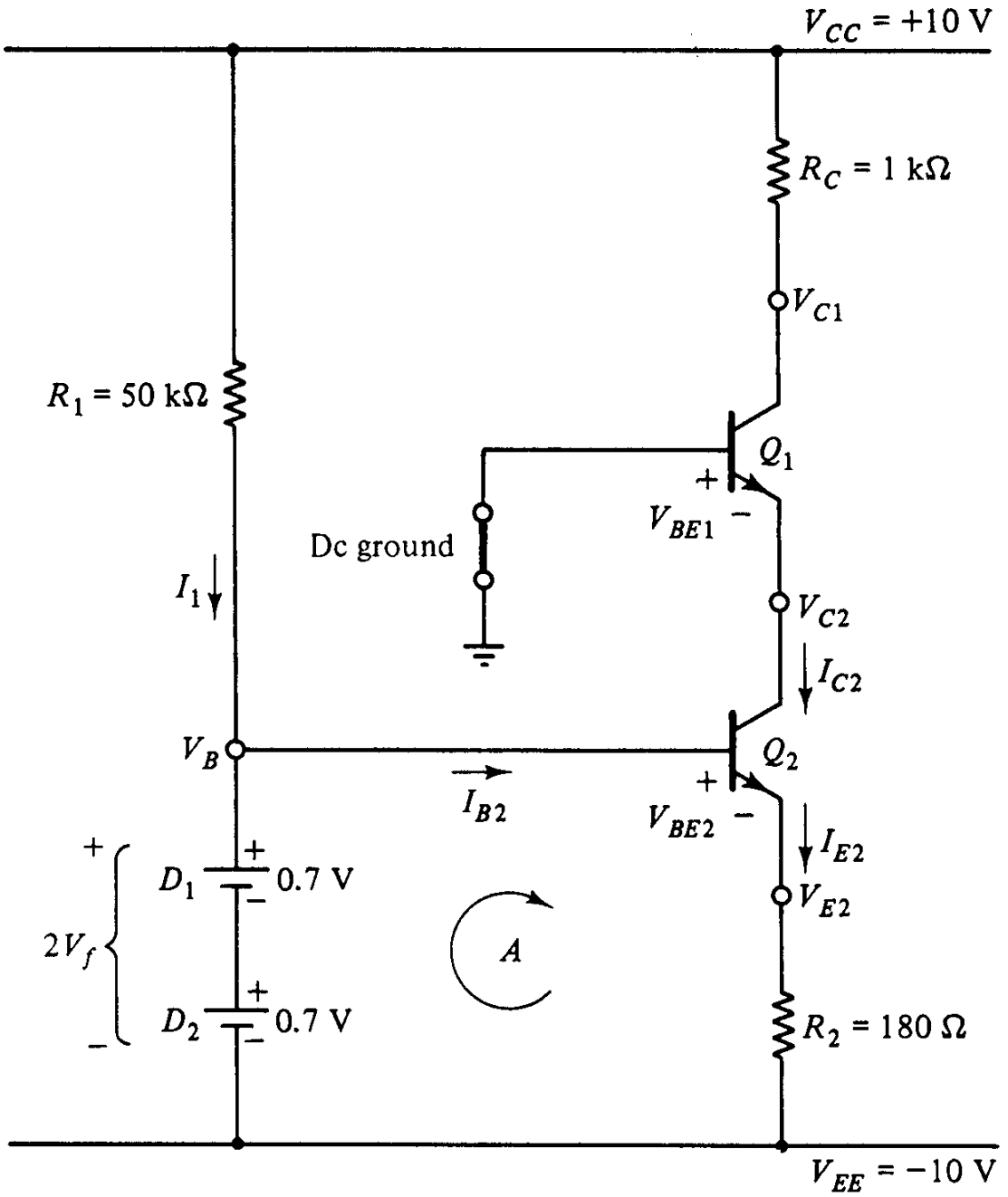


Figure 7.35
Equivalent bias circuit of Fig. 7.34.



Problem: For the previous circuits find the bias values I_C and V_{CE} for each transistor

Solution

Assume D_1 and D_2 forward biases ($I_1 > I_{B2}$)

$$V_B = V_{EE} + 2V_F = -10\,\text{V} + 2(0.7\,\text{V}) = -8.6\,\text{V}$$

Using KVL around loop A

$$2V_F = V_{BE2} + I_{E2}R_2$$

Since $V_{BE2} \cong V_F$

$$I_{E2} = \frac{V_F}{R_2} = \frac{0.7\,\text{V}}{180\,\Omega} \cong 3.7\,\text{mA}$$

Since $I_C \cong I_E$

$$I_{C1} = I_{C2} = 3.9\,\text{mA}$$

Check that D_1 and D_2 are forward biased for a worst case minimum $\beta_F = 20$

$$I_{B2} = \frac{I_{C2}}{\beta_F} \cong 0.19\,\text{mA}$$

$$I_1 = \frac{V_{CC} - V_B}{R_1} = \frac{10\,\text{V} - (-8.6\,\text{V})}{50\,\text{k}\Omega} = 0.37\,\text{mA}$$

$$V_{C1} = V_{CC} - I_{C1}R_C = 10\,\text{V} - (3.9\,\text{mA})(1\,\text{k}\Omega) = 6.1\,\text{V}$$

$$V_{E2} = V_B - V_{BE2} = -8.6\,\text{V} - 0.7\,\text{V} = -9.3\,\text{V}$$

$$V_{E1} = V_{C2} = 0\,\text{V} - V_{BE1} = -0.7\,\text{V}$$

$$V_{CE1} = V_{C1} - V_{E1} = 6.1\,\text{V} - (-0.7\,\text{V}) = 6.8\,\text{V}$$

$$V_{CE2} = V_{C2} - V_{E2} = -0.7\,\text{V} - (-9.3\,\text{V}) = 8.6\,\text{V}$$

Current Mirrors

- Current mirrors also take advantage of matched transistors but require a minimal number of resistors. They are also well suited for circuits with more than one stage.

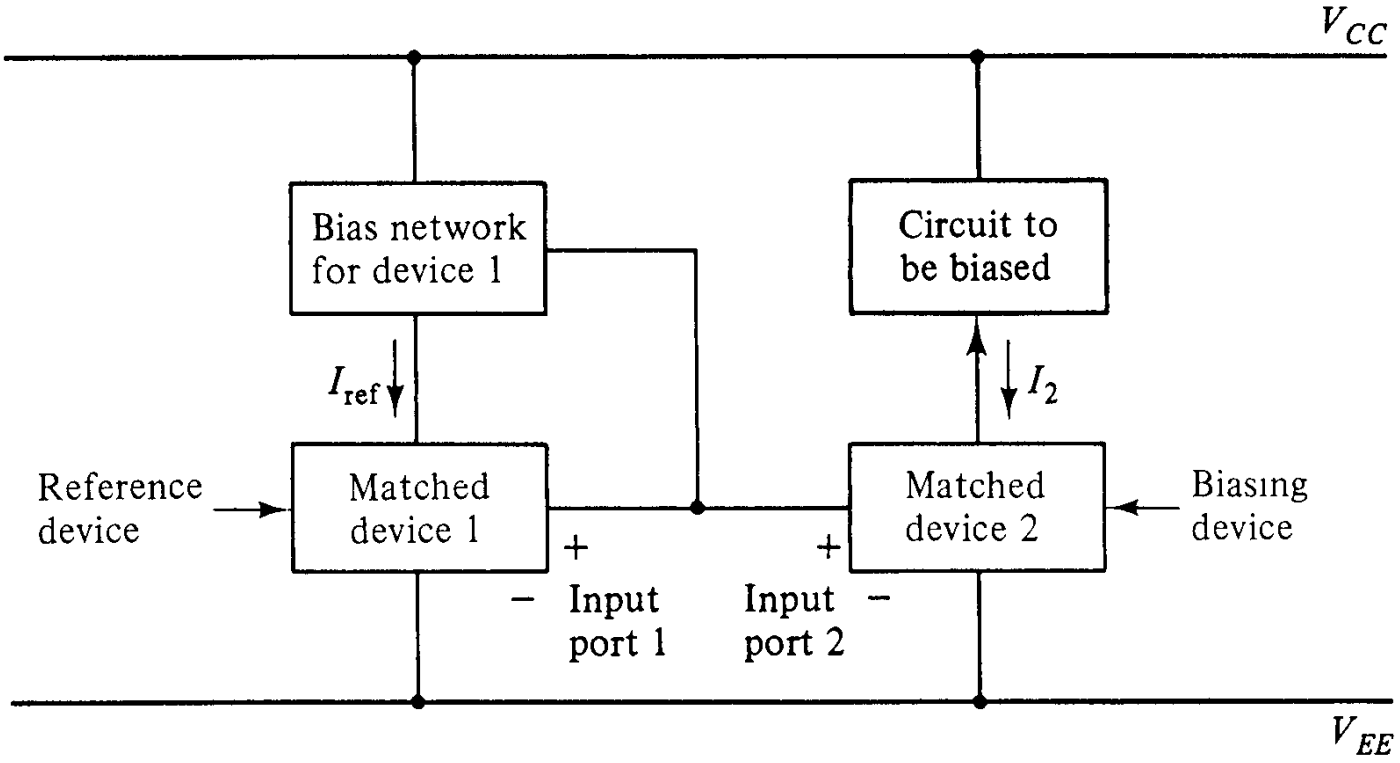
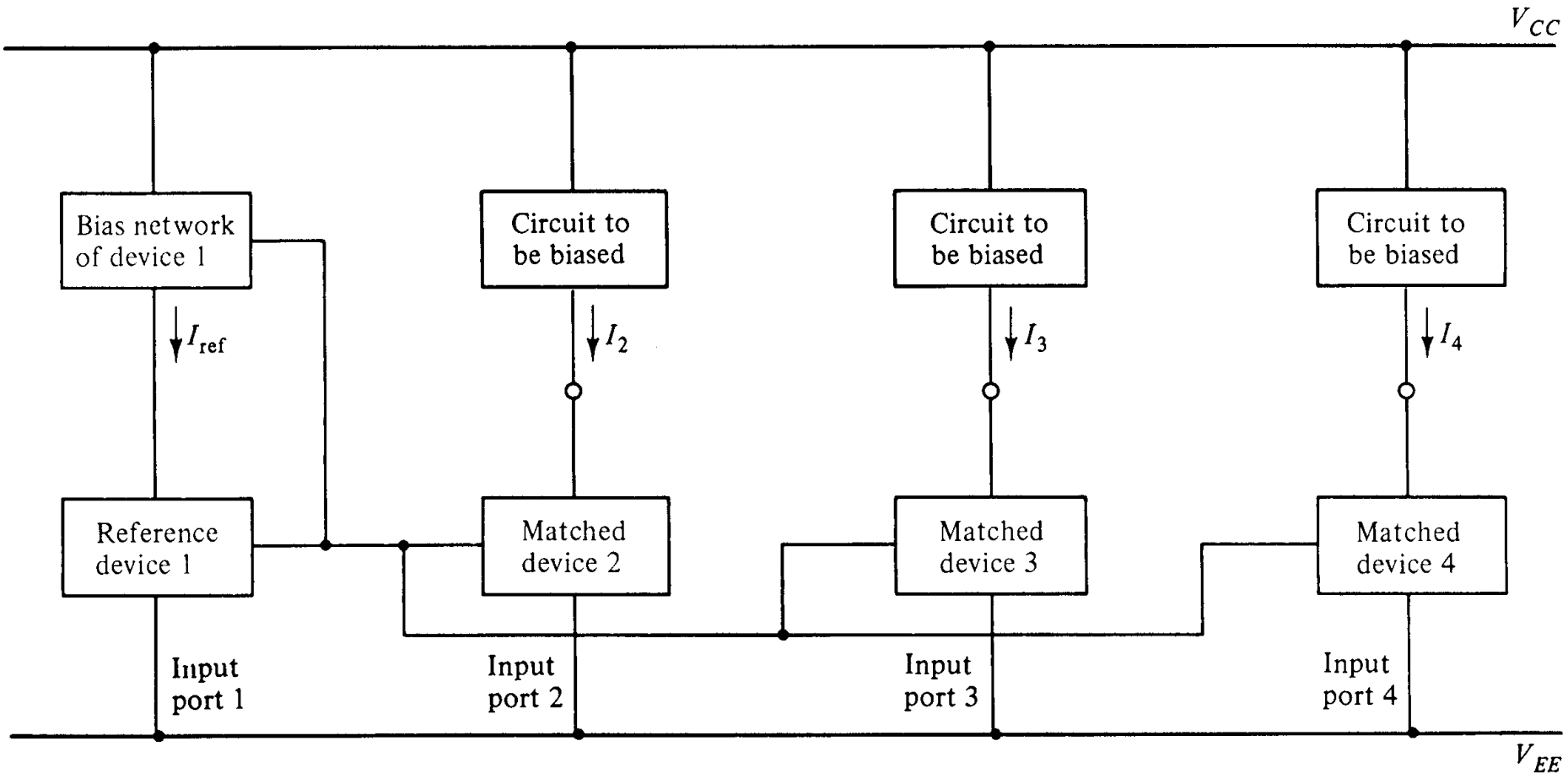


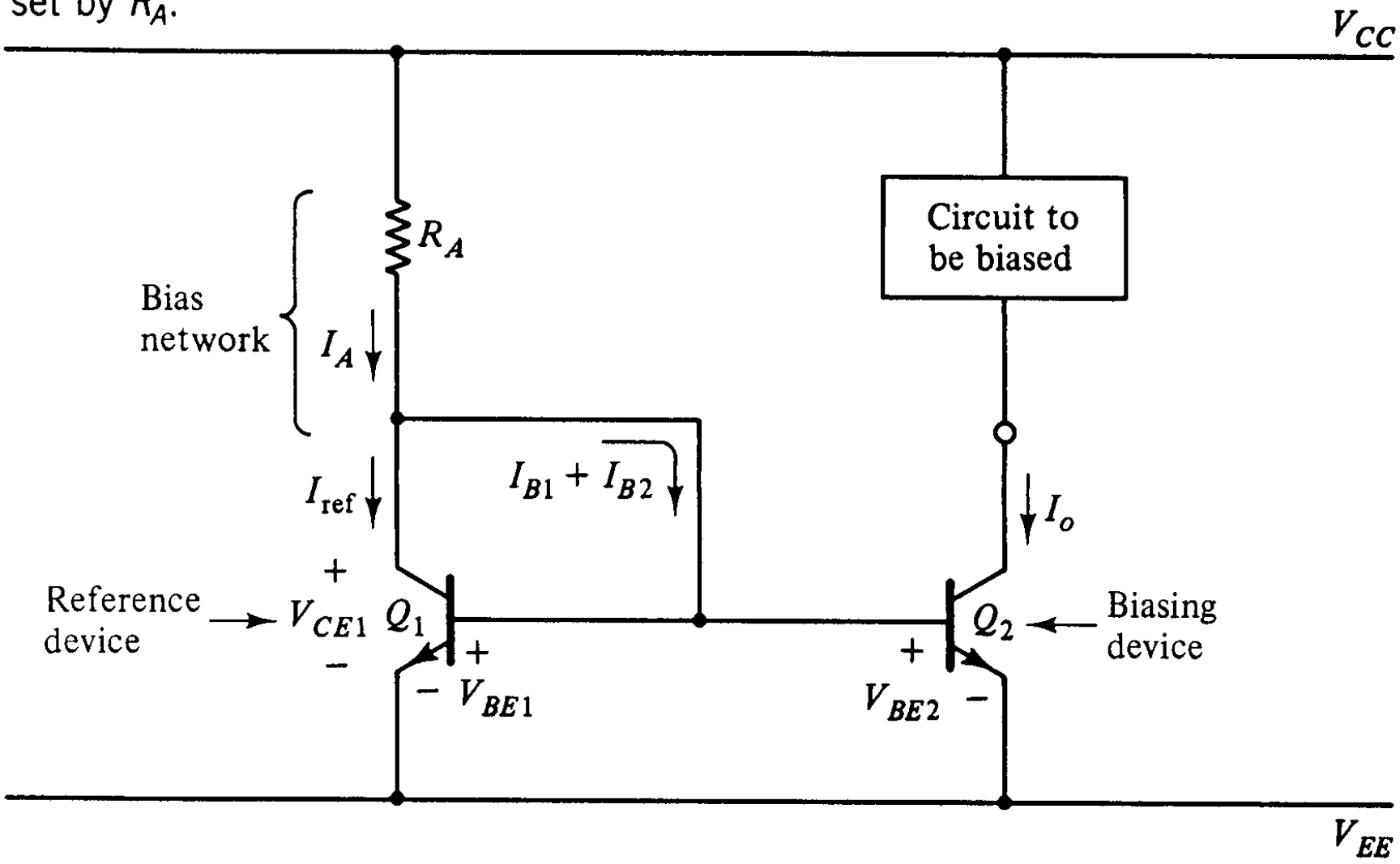
Figure 7.39
Basic topology of the current mirror bias circuit. The biasing device is perfectly matched to the reference device, through which the reference current I_{ref} is established.

Figure 7.40 Three circuits biased by a common current mirror reference.



Basic BJT Current Mirror

Figure 7.41
BJT current mirror bias circuit. The current I_{ref} is set by R_A.



$$I_A = \frac{V_{CC} - (V_{CE1} + V_{EE})}{R_A} = \frac{V_{CC} - V_{BE1} - V_{EE}}{R_A}$$

$$I_A = I_{REF} + I_{B1} + I_{B2}$$

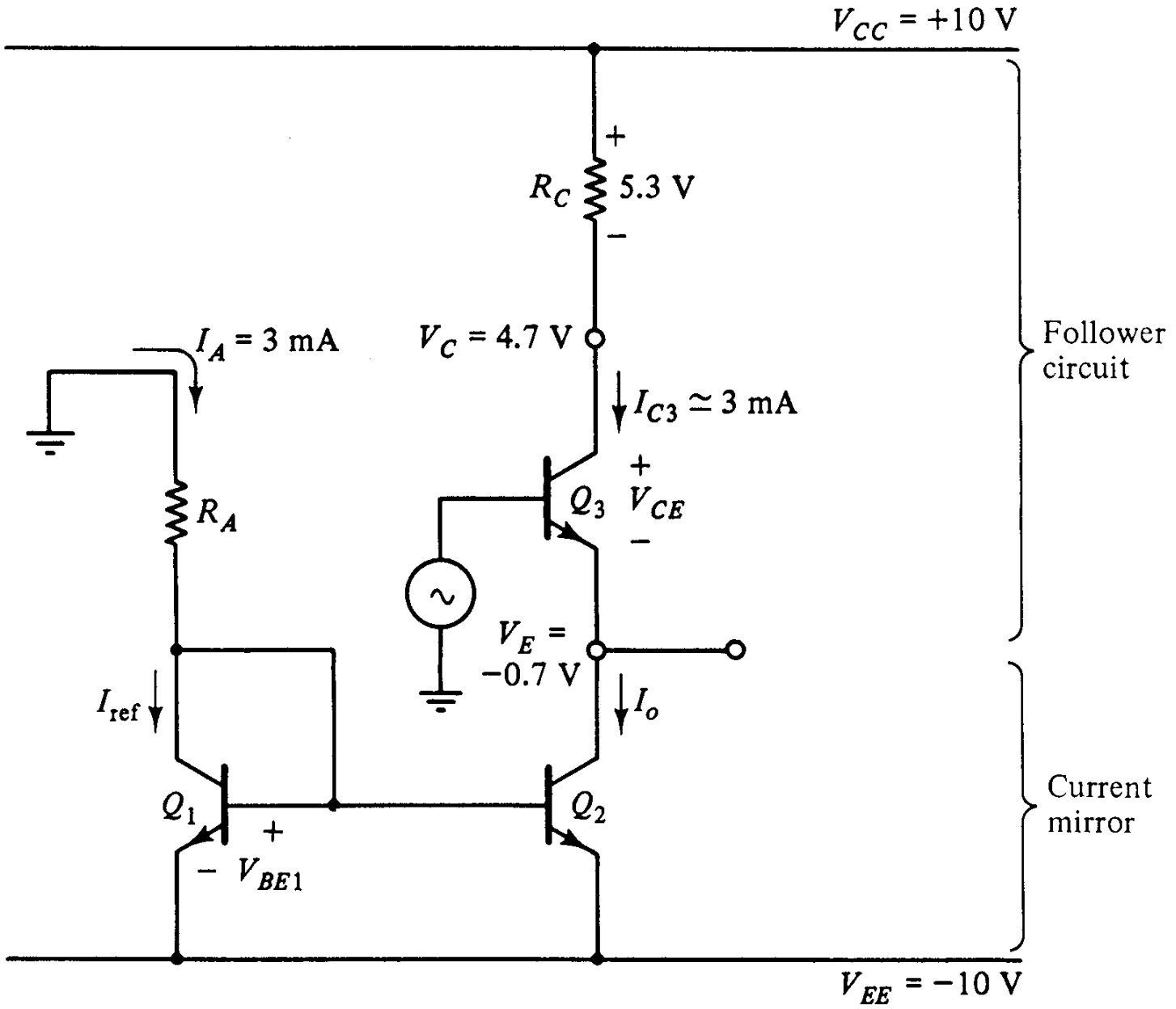
IF β_F is large $I_{B1} << I_{REF}$ $\quad$ $I_{B2} << I_{REF}$

$$I_{REF} \cong I_A$$

Problem

For the following circuit I_{C3} = 3 mA and V_{CE} = 5.4 V. Find the quiescent (DC bias) power dissipated in each transistor.

Figure 7.42
Current mirror bias circuit design example.



$$I_{C3} \cong I_o = I_{REF} \cong I_A$$

$$I_A = \frac{0\,\text{V} - (V_F + V_{EE})}{R_A}$$

$$R_A = \frac{-V_F - V_{EE}}{I_{REF}} = \frac{-0.7\,\text{V} - (-10\,\text{V})}{3\,\text{mA}} = 3.1\,\text{k}\Omega$$

$V_E = -0.7\,\text{V}$; To achieve $V_{CE} = 5.4\,\text{V}$, $V_C = 4.7\,\text{V}$

$$V_{CC} - V_C = 10\,\text{V} - 4.7\,\text{V} = 5.3\,\text{V}$$

$$R_C = \frac{5.3\,\text{V}}{3\,\text{mA}} = 1.8\,\text{k}\Omega$$

The DC power in each transistor is given by:

$$P_Q = I_C V_{CE} + I_B V_{BE} \cong I_C V_{CE}$$

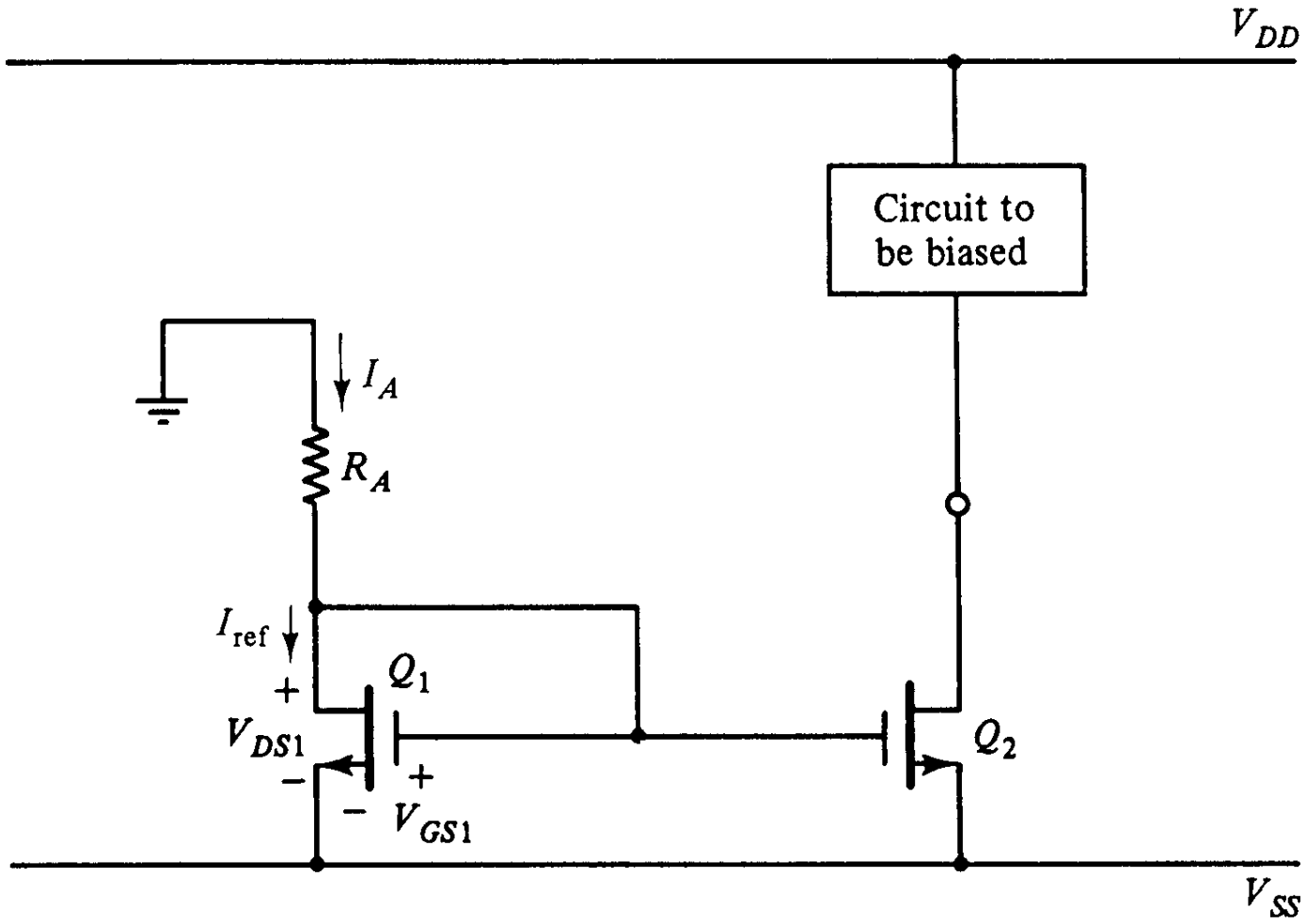
$$P_{Q1} = (3\,\text{mA})(0.7\,\text{V}) = 0.2\,\text{mW}$$

$$P_{Q2} = (3\,\text{mA})[-0.7\,\text{V} - (-10\,\text{V})] \cong 28\,\text{mW}$$

$$P_{Q3} = (3\,\text{mA})(5.4\,\text{V}) = 16\,\text{mW}$$

MOSFET Current Mirror

Figure 7.44
MOSFET current mirror made from matched devices. The reference current is determined by R_A, K, and V_{TR}.



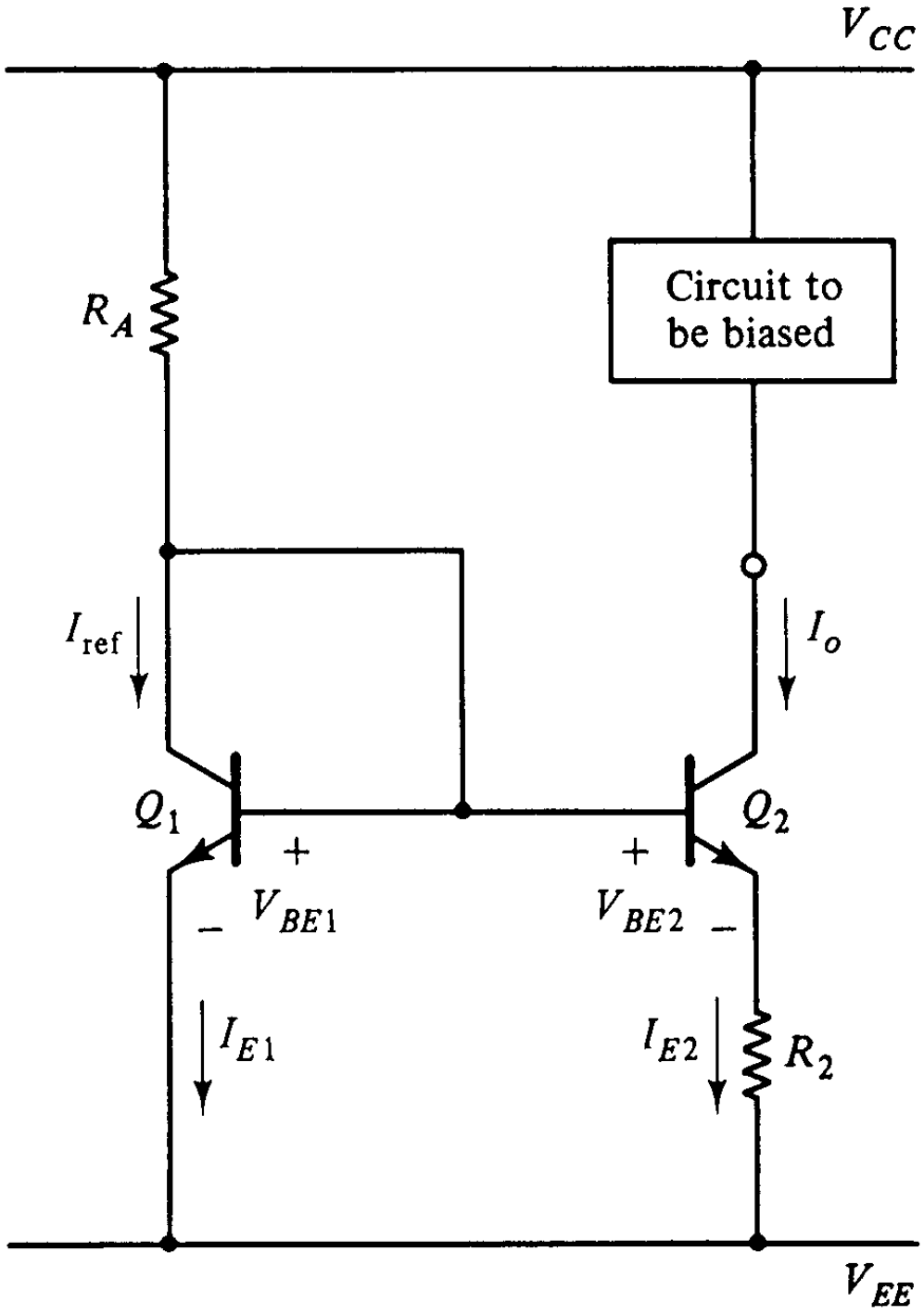
Advantage: $I_{REF} = I_A$

Gate current is negligible

Widlar Current Source

- The basic current mirror requires that the bias current and reference current be equal
- The wildar current source sets the mirrored current to a value smaller than I_{REF} by using an extra resistor
- The widlar current source allows you to establish small bias currents (μA) without using large resistor values

Figure 7.46
Widlar current source.



$$I_{REF} \cong \frac{V_{CC} - V_{EE} - V_{BE1}}{R_A}$$

$$V_{BE1} = V_{BE2} + I_{E2} R_2$$

$$I_E = I_{EO}\left(e^{V_{BE} / \eta V_T} - 1 \right) \cong I_{EO}\, e^{V_{BE} / \eta V_T}$$

$$V_{BE} = \eta V_T \ln \frac{I_E}{I_{EO}}$$

Assuming matched BJTs

$$\eta V_T \ln \frac{I_{E1}}{I_{EO}} = \eta V_T \ln \frac{I_{E1}}{I_{EO}} + I_{E2} R_2$$

$$I_{E2} R_2 = \eta V_T \ln \frac{I_{E1}}{I_{E2}}$$

$$I_{E1} \cong I_{REF} \qquad I_{E2} \cong I_o$$

$$I_o = \frac{\eta V_T}{R_2} \ln \frac{I_{REF}}{I_o}$$

- Equation difficult to solve in closed form. Use successive iteration or trial and error
- When you know the desired I_o then I_{REF} can be found directly

$$I_{REF} = I_o \exp\left(\frac{I_o R_2}{\eta V_T}\right)$$

Problem:

Using a widlar current source find the values of R_A and R_B that will produce I_o = 100 μA. Given V_{CC} = 10 V, VEE = -10 V, V_F = 0.7 V and η = 1.

Solution:

Select a value of R_2 such that

$$I_o R_2 \cong \eta V_T$$

To keep exponent from becoming too large

$$\eta V_T = 25\,\text{mV}$$

Choose $I_o R_2 = 100\,\text{mV} \quad \therefore \; R_2 = 1\,\text{k}\Omega$

$$I_{REF} = (100\,\text{mA})\exp\left[\frac{(100\,\text{mA})(1\,\text{k}\Omega)}{0.025\,\text{V}}\right] = 5.46\,\text{mA}$$

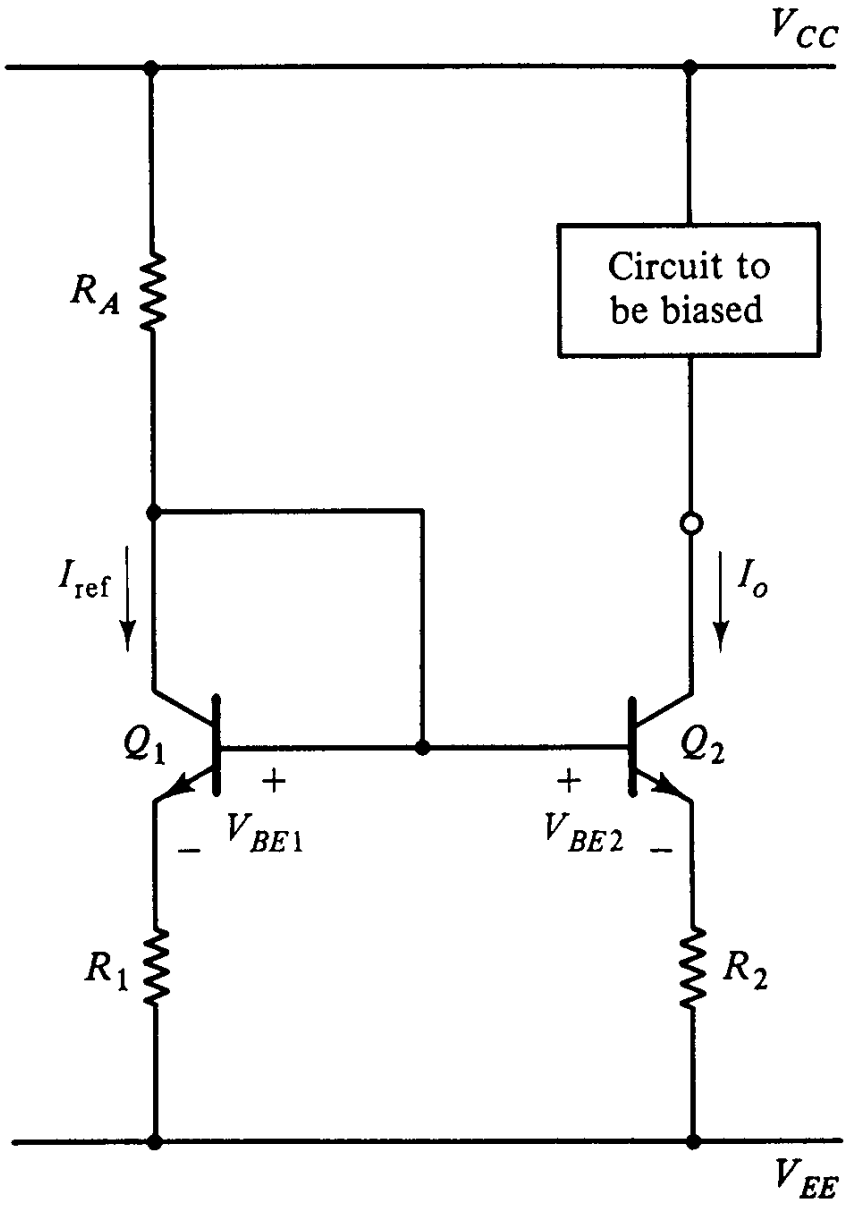
$$I_{REF} = \frac{V_{CC} - V_{EE} - V_F}{R_A}$$

$$R_A = \frac{10\,\text{V} - (-10\,\text{V}) - 0.7\,\text{V}}{5.46\,\text{mA}} = 3.54\,\text{k}\Omega$$

Wilson Current Source

- Refined Widlar source that can produce $I_O > I_{REF}$

Figure 7.48
Refined version of the Widlar current source, called the Wilson current source.



- The balance between V_{BE1} and V_{BE2} is set by the ratio of R_1 to R_2

Assuming $I_C \cong I_E$

$$V_{BE1} + I_{REF} R_1 = V_{BE2} + I_o R_2$$

$$\eta V_T \ln \frac{I_{REF}}{I_{EO1}} + I_{REF} R_1 = \eta V_T \ln \frac{I_o}{I_{EO2}} + I_o R_2$$

Assuming matched devices

$$I_o = \frac{\eta V_T}{R_2} \ln \frac{I_{REF}}{I_o} + I_{REF} \frac{R_1}{R_2}$$

Small Signal Modeling of Three Terminal Devices

- Incremental signals
- Piecewise linear models
- Incremental circuit models
  - BJT
  - FET
- Refinements to incremental model
  - Output resistance
  - Input resistance
  - Alternative BJT representation
- Two - port representations

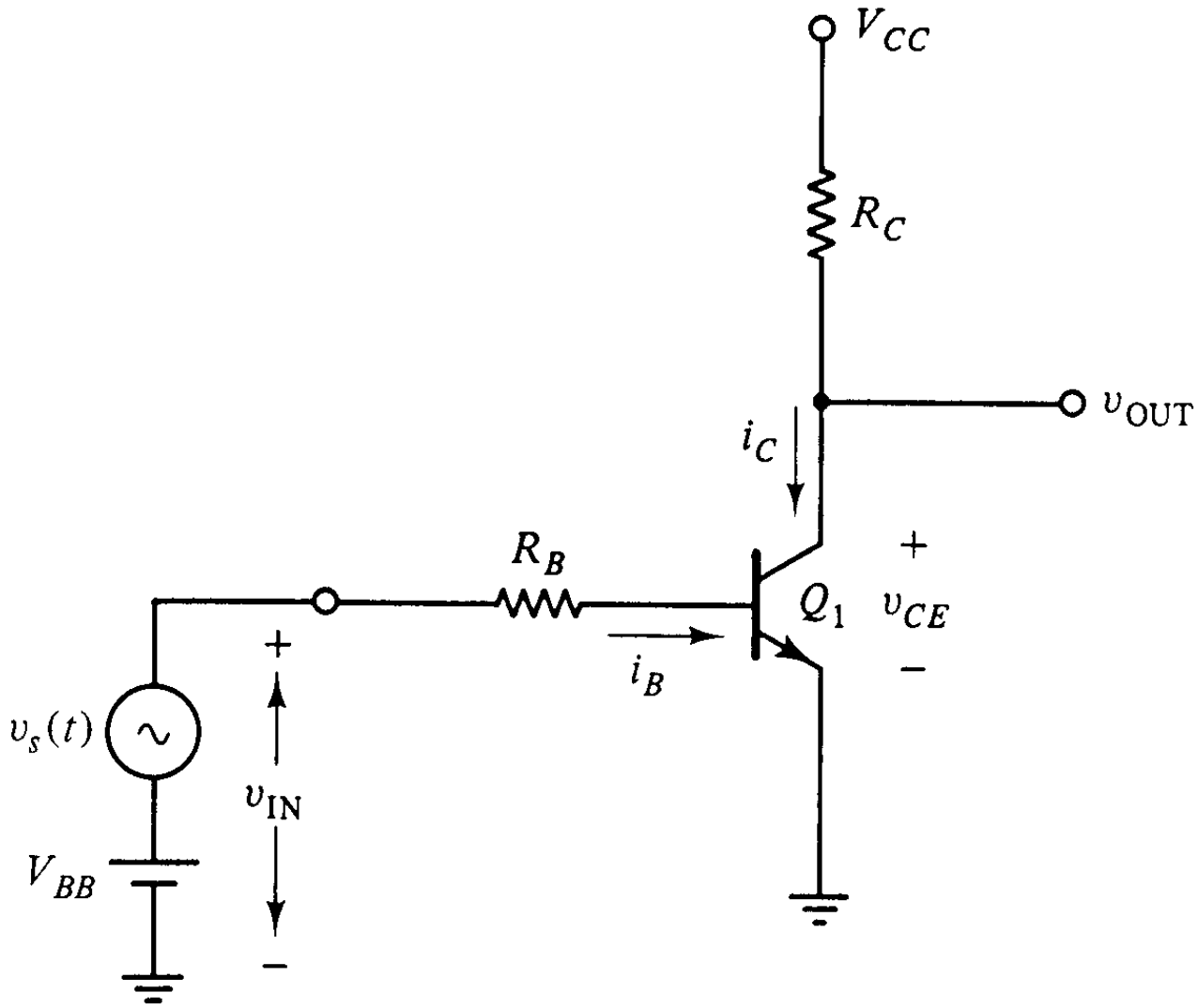
Small Signal Modeling of Three Terminal Devices

- Related to PWL concept in which the V-I characteristics are modeled by a straight line tangent to the curve at a particular operating point
- With three terminal devices the relationship between the output port and input port must be taken into account. This generally leads to a PWL model with a linearly dependent source.
- Circuits containing small signal models can be analyzed using linear circuit theory under proper conditions
- The terms small-signal and incremental will be used interchangeably

Incremental Signals

- Any transient, periodic or AC fluctuation in a voltage or current
- An incremental signal is small in magnitude compared to the bias voltages or currents in the circuit
- Incremental signal carries the signal information processed by the circuit

Figure 8.1
Simple BJT inverter with input equal to a bias voltage V_{BB} plus incremental signal voltage v_s.



$$\begin{array}{lcccl} v_{\text{IN}} & = & V_{BB} & + & v_s(t) \\ \text{total} & = & \text{bias} & + & \text{incremental} \\ \text{voltage} & & \text{component} & & \text{signal} \end{array} \tag{8.1}$$

The signal and bias portions of the input voltage are responsible for the corresponding components of the circuit's output voltage or current. For the inverter of Fig. 8.1, the output voltage can be expressed by

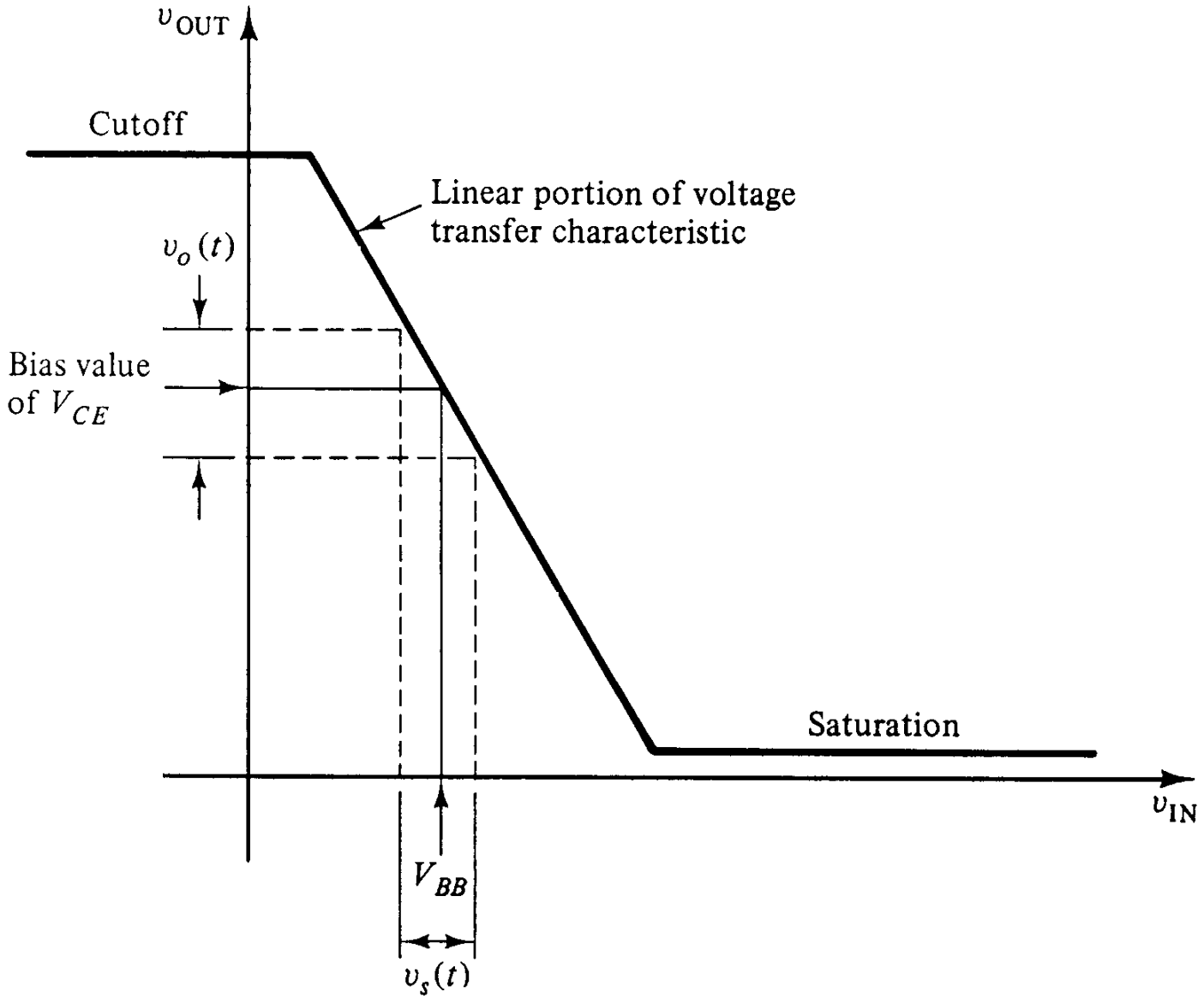
$$v_{\text{OUT}} = V_{CE} + v_o(t) \tag{8.2}$$

where V_{CE} is the bias component and $v_o(t)$ the signal component. The bias component V_{CE} is established by V_{BB}, while the signal component $v_o(t)$ is driven by $v_s(t)$. Similarly, the collector and base currents in the BJT can be expressed as

$$i_C = I_C + i_c(t) \qquad \text{and} \qquad i_B = I_B + i_b(t) \tag{8.3}$$

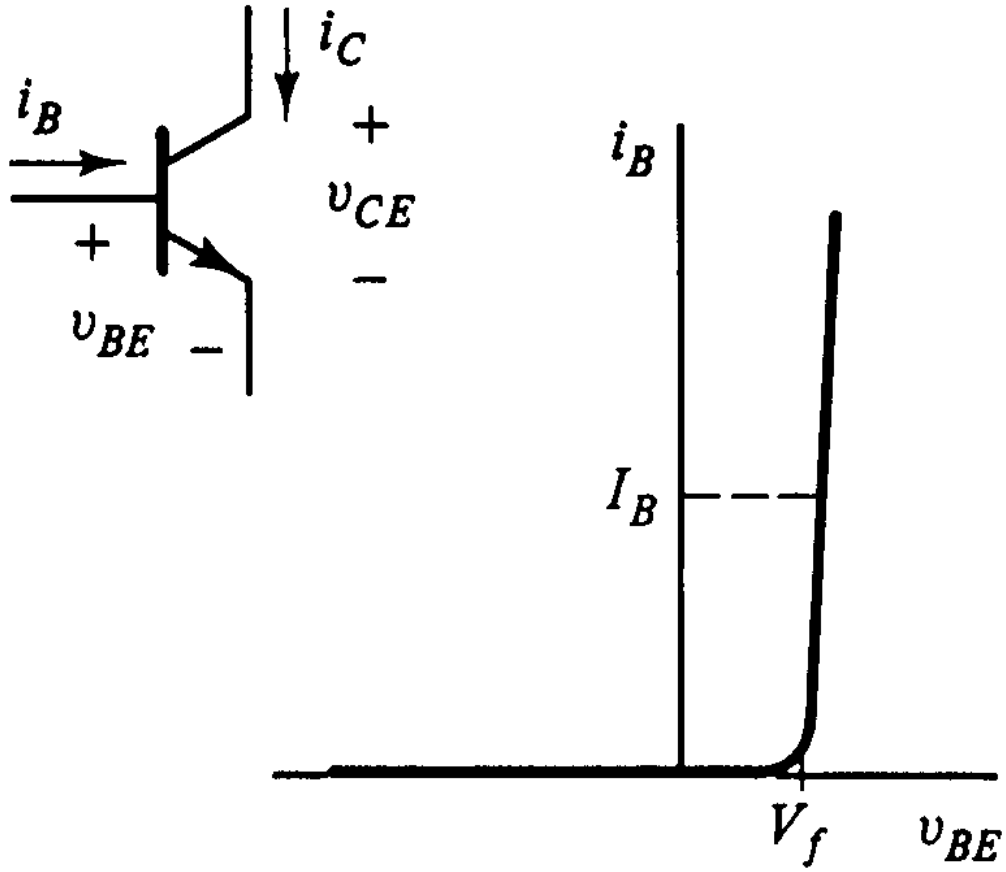
The bias components I_C and I_B are established by V_{BB}, and the incremental components $i_c(t)$ and $i_b(t)$ are driven by $v_s(t)$.

Figure 8.2
Bias plus incremental signal component applied to BJT inverter voltage transfer characteristic.



PWL Models of Three Terminal Devices

- Formation of small signal model begins with PWL model
- PWL model can be applied to three terminal device if the dependency of the output port is considered



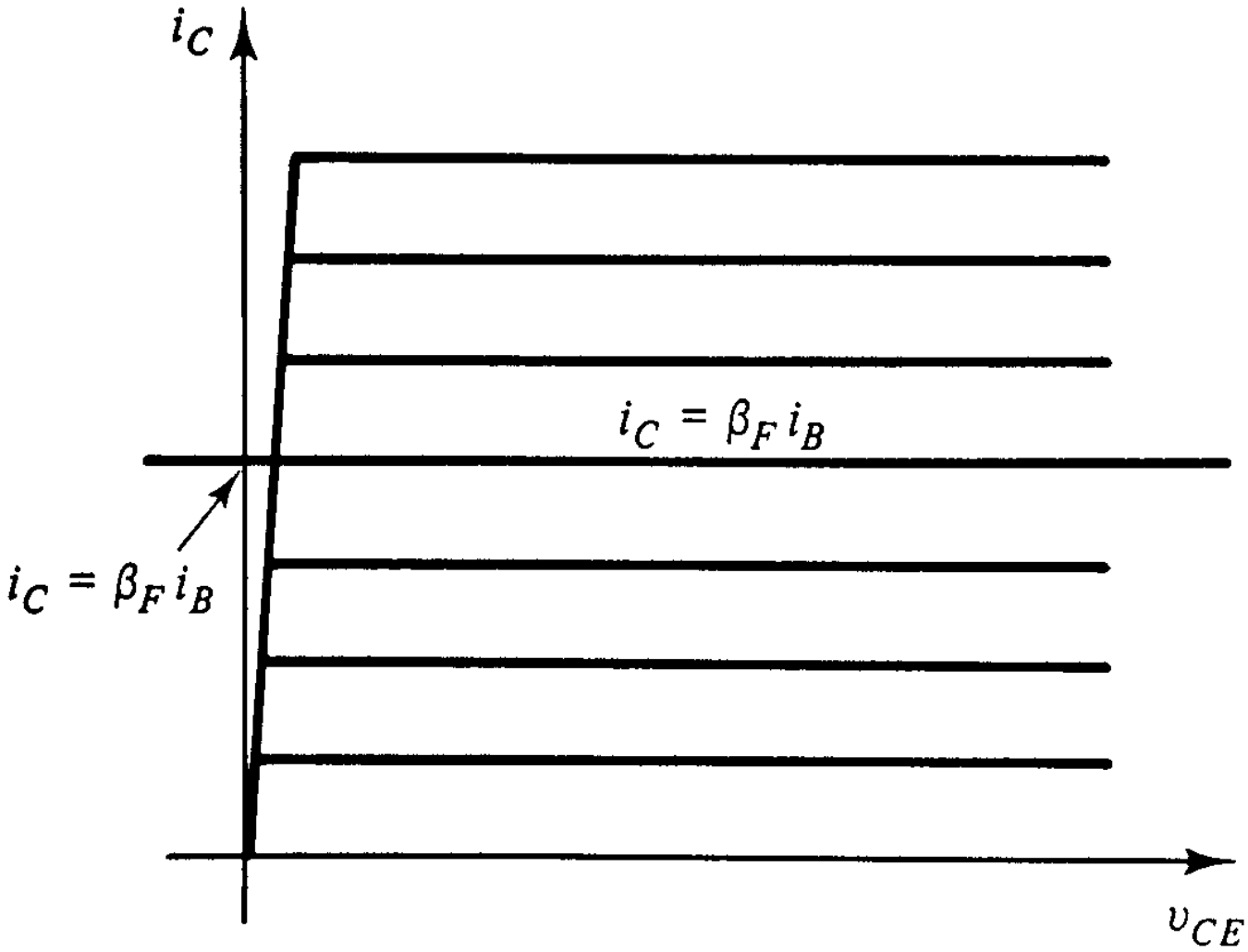
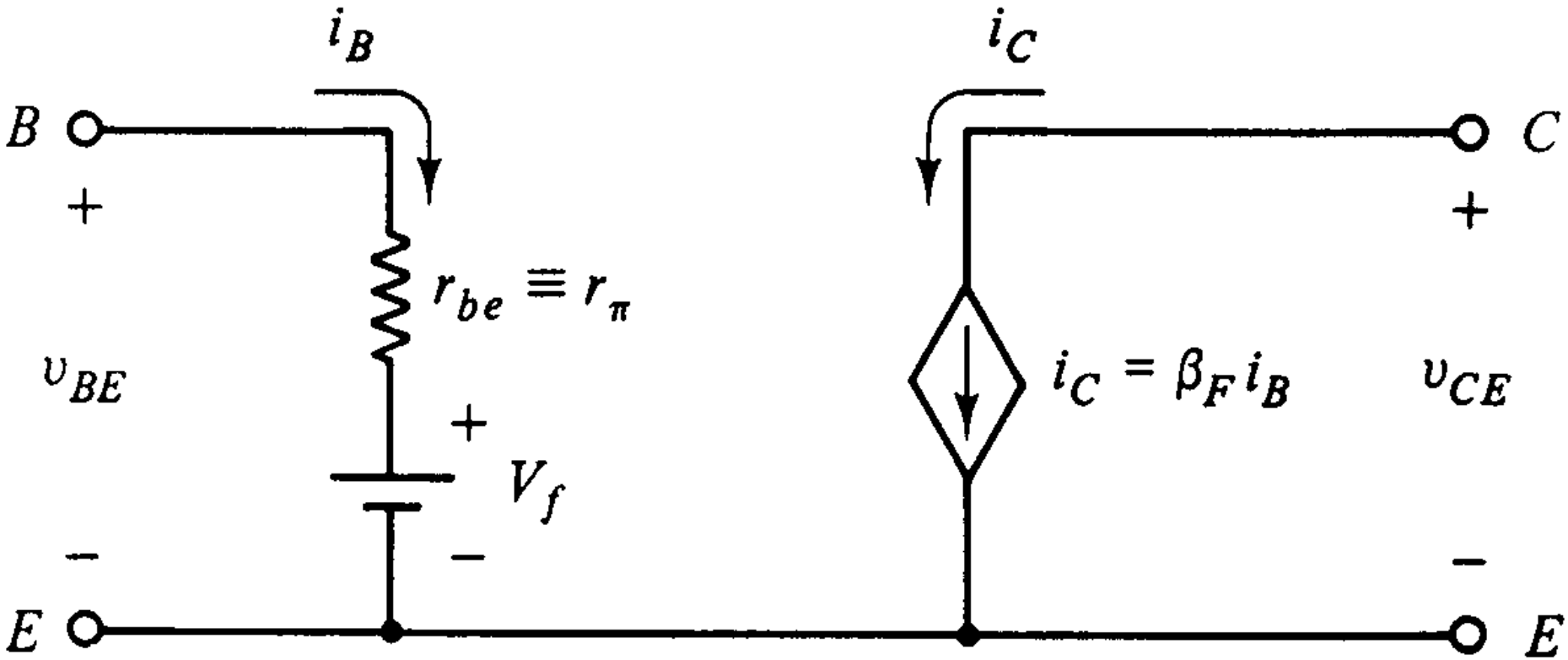


Figure 8.3
(a) Voltage–current characteristic of the base–emitter input port of a BJT resembles the *v–i* characteristic of the PN junction diode; (b) idealized BJT output port *v–i* characteristic. The finite upward slope in the active region has been assumed negligible in this figure.

Figure 8.4
Piecewise linear model of the BJT with both ports represented.



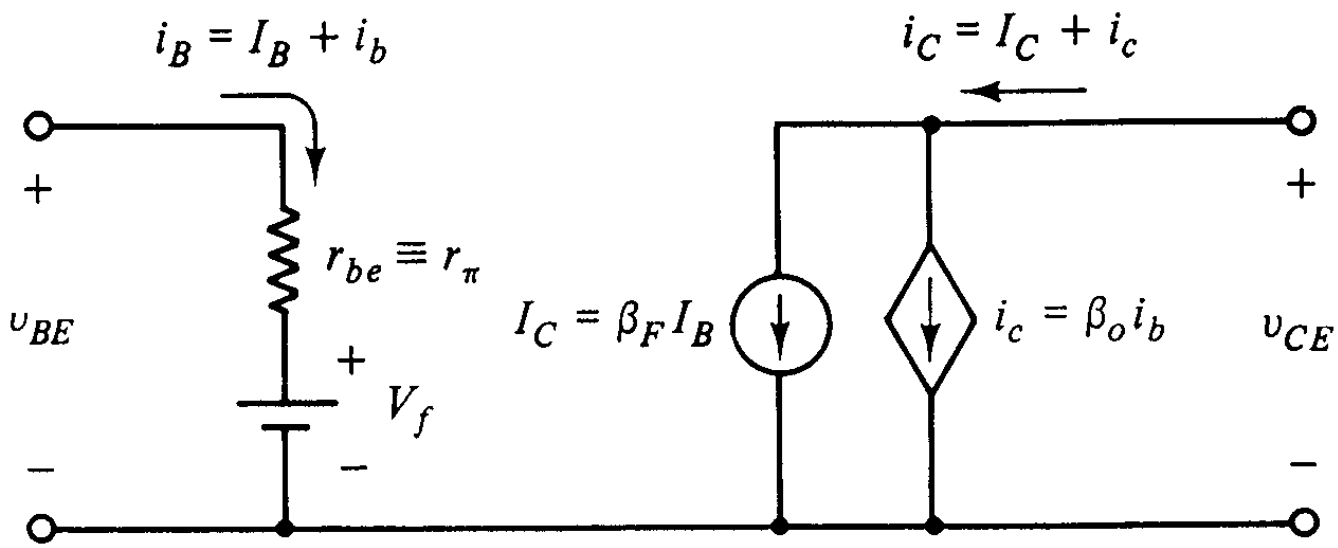
$$r_{BE} = \left. \frac{\partial v_{be}}{\partial i_b} \right|_{V_{BE}, I_B} = \frac{\eta V_T}{I_B}$$

- Model valid only in constant current region
- If the circuit in which the BJT is connected produces a signal as well as a bias component to i_B then:

$$i_c(t) = \beta_o \, i_b(t)$$

- where i_c and i_b are inc
- remental signals and β_o is the incremental current gain

Piecewise linear model for the BJT in which the dc portion I_C of the collector current is related to I_B via β_F, and the incremental signal portion i_c of the collector current is related to i_b via β_o. The input port is modeled by V_f and r_{be}.



- Since β_F is fairly constant it is possible to assume $\beta_o = \beta_F$ in many cases
- The symbols h_{FE} and h_{fe} are sometimes used instead of β_F and β_o when using h-parameter analysis

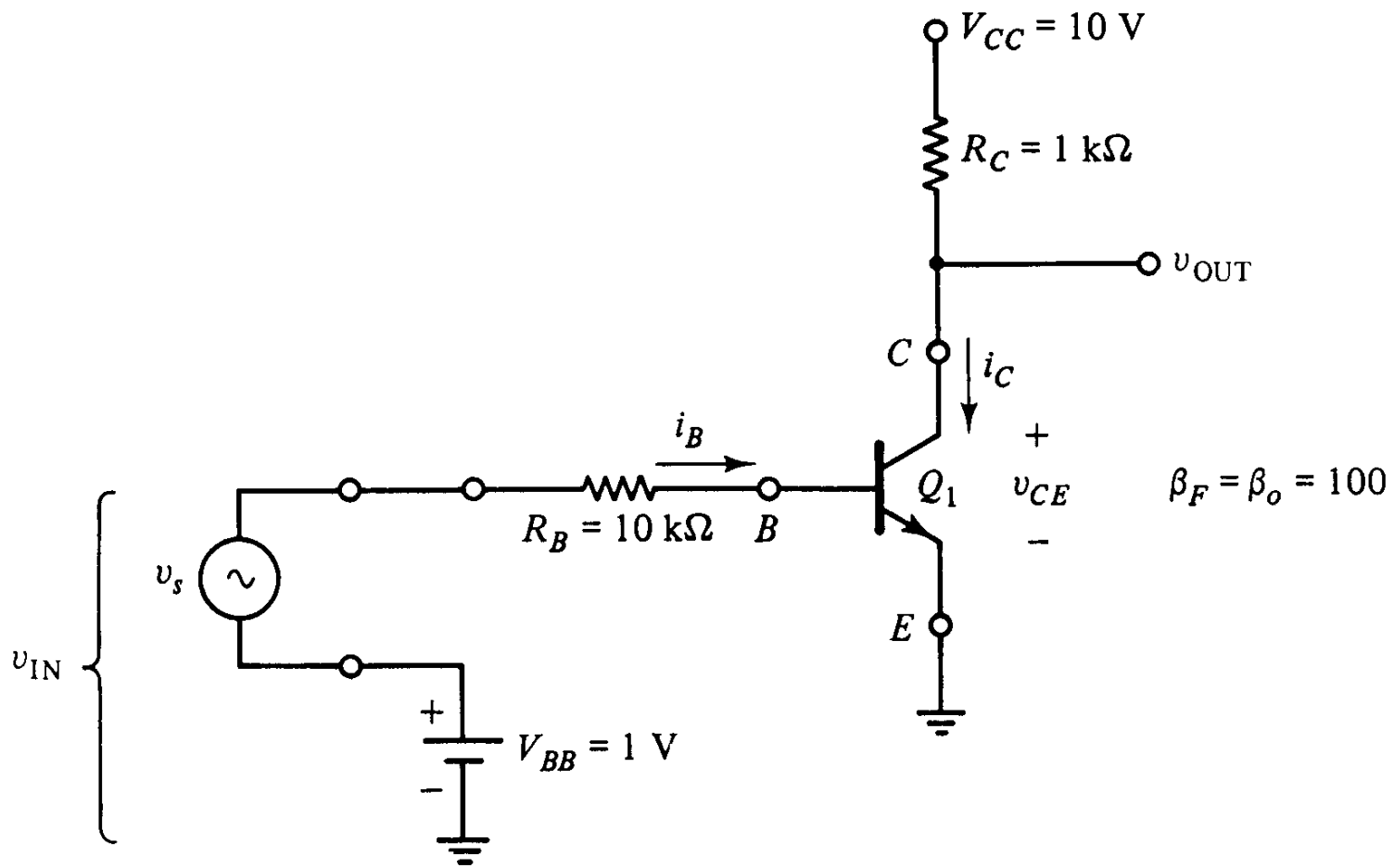
Incremental Circuit Model

In analyzing the small signal performance of a circuit it is customary to ignore the DC components of the model once the bias conditions have been established.

This can be accomplished by the following procedure:

1. Find the DC bias point and determine an appropriate PWL model
2. Set all bias values to zero by setting all DC sources to zero (including those in the PWL model)
3. Solve the desired variables using linear circuit theory
4. Superimpose the signal variables onto the corresponding DC bias voltages and currents to obtain the total voltage and current values

Figure 8.7
Simple BJT inverter with the transistor biased in its active region by V_{BB}. The voltage v_s is the signal component of the total input voltage v_{IN}.



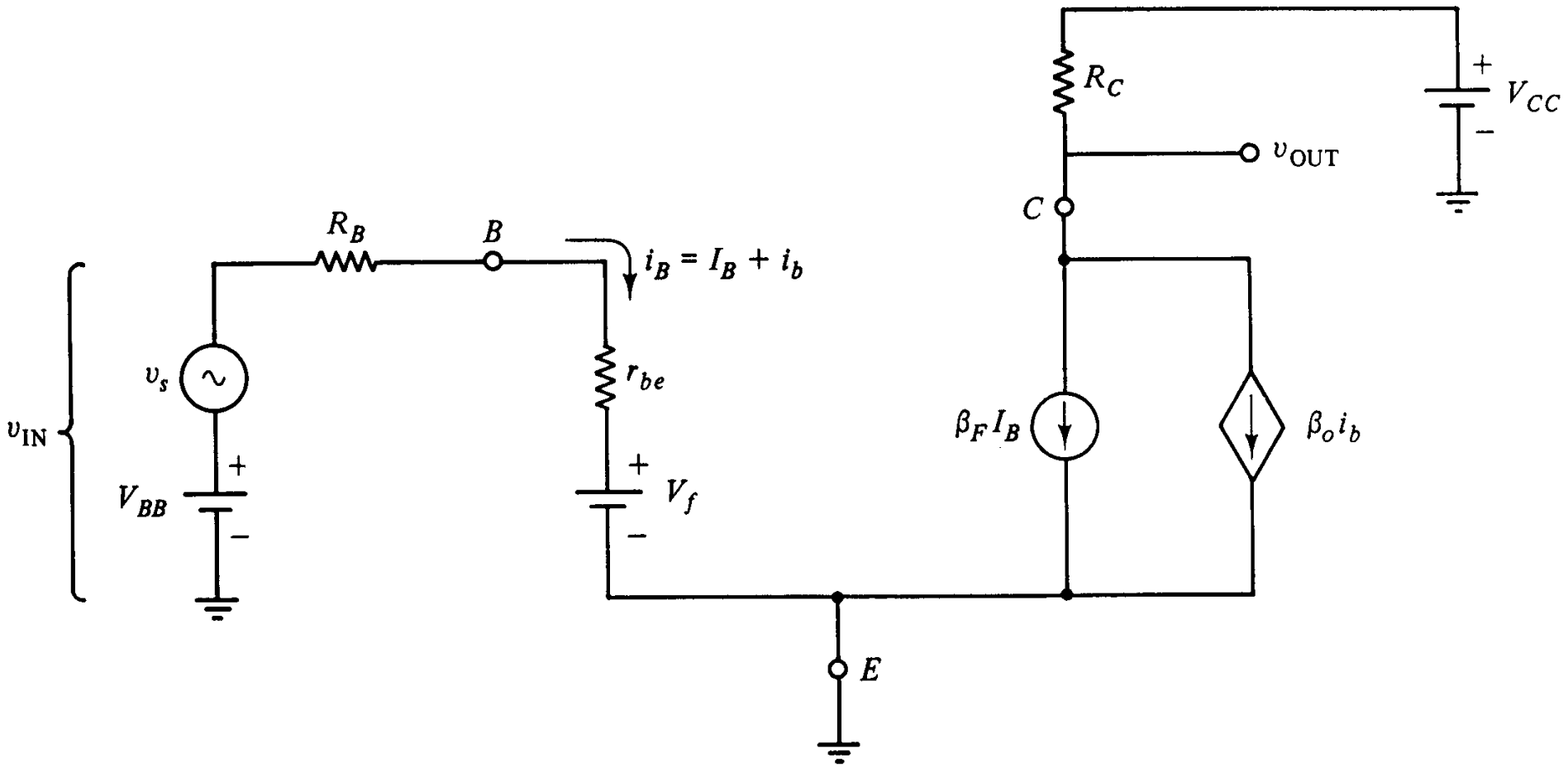


Figure 8.8 Constant-current-region piecewise linear model substituted for the BJT in the circuit of Fig. 8.7.

$$I_B = \frac{V_{BB} - V_F}{R_B} = \frac{1\,\text{V} - 0.7\,\text{V}}{10\,\text{k}\Omega} = 30\,\mu\text{A}$$

$$I_C = \beta_F I_B = (100)(30\,\mu\text{A}) = 3\,\text{mA}$$

$$V_{OUT} = V_{CE} = V_{CC} - I_C R_C = 10\,\text{V} - (3\,\text{mA})(1\,\text{k}\Omega) = 7\,\text{V}$$

- Transistor operates in constant current therefore we can use PWL model developed earlier

$$r_{be} = \frac{\eta V_T}{I_B} = \frac{1(0.025)}{30\,\mu\text{A}} \cong 833\,\Omega$$

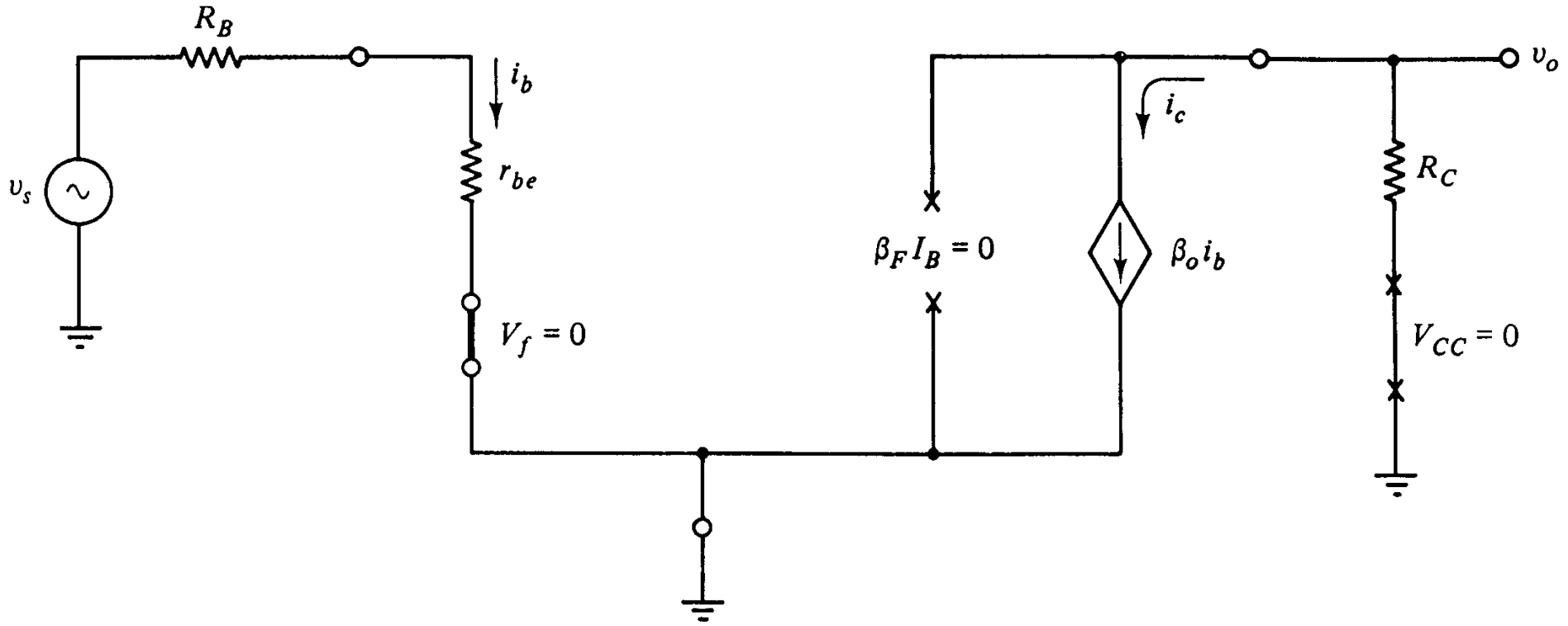


Figure 8.9 Incremental representation of the circuit of Fig. 8.7.

$$i_b = \frac{v_s}{R_B + r_{be}} \qquad v_o = -\beta_o i_b R_C$$

$$v_o = \frac{-\beta_o R_C}{R_B + r_{be}} v_s = \frac{-100(1\,\text{k}\Omega)}{10\,\text{k}\Omega + 0.833\,\text{k}\Omega} v_s \cong -9.2\, v_s$$

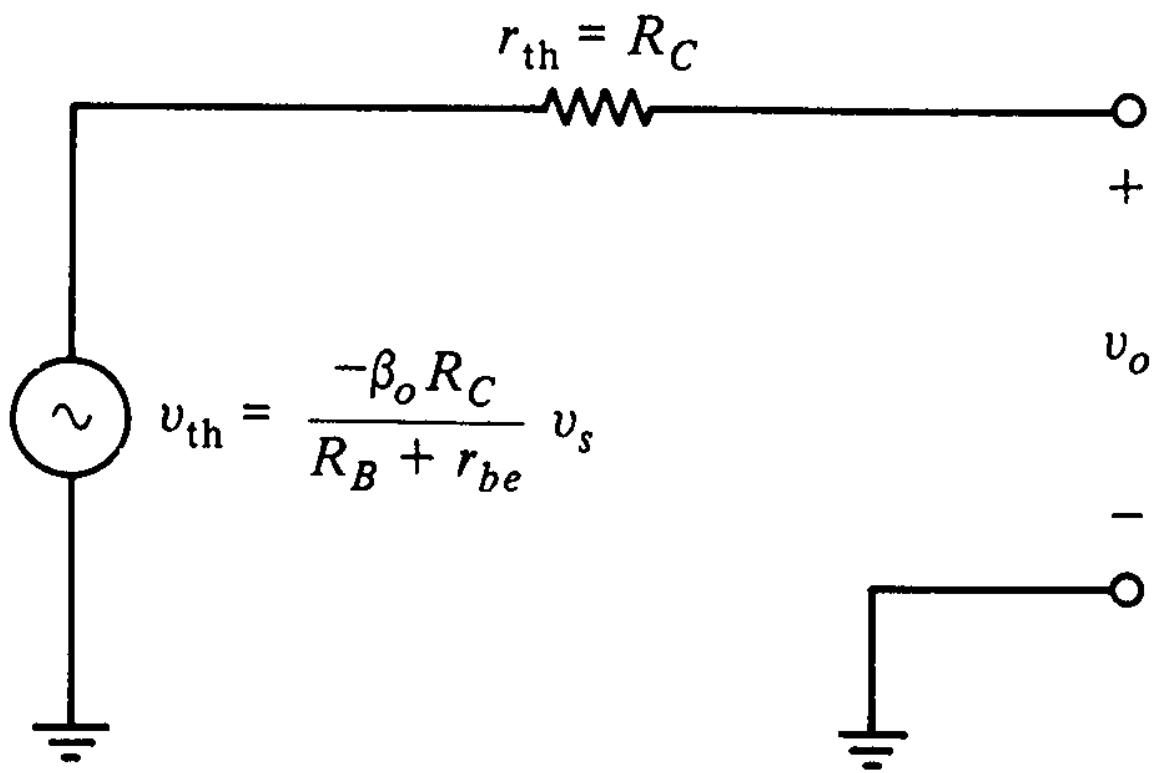
$\frac{-\beta_o R_C}{R_B + r_{be}}$ is the incremental or small-signal voltage gain

$$V_{OUT} = V_{CE} + v_o(t) = 7\,\text{V} - 9.2\, v_s(t)$$

Total = Bias + Incremental

Voltage Voltage Signal

Figure 8.11
Thévenin equivalent of the output port of the circuit of Fig. 8.9.



Problem:

For the following circuit find the incremental components of v_c and v_e.

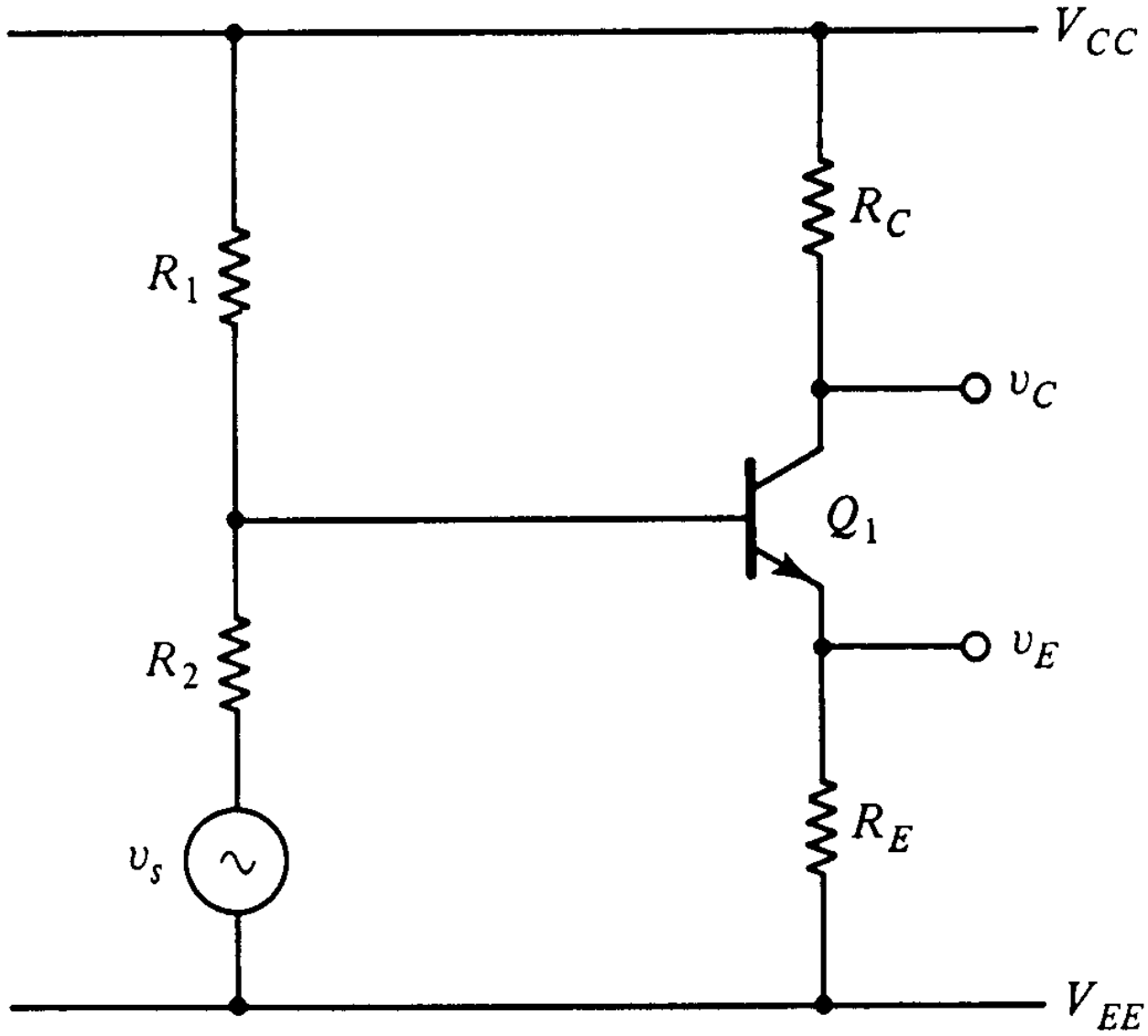
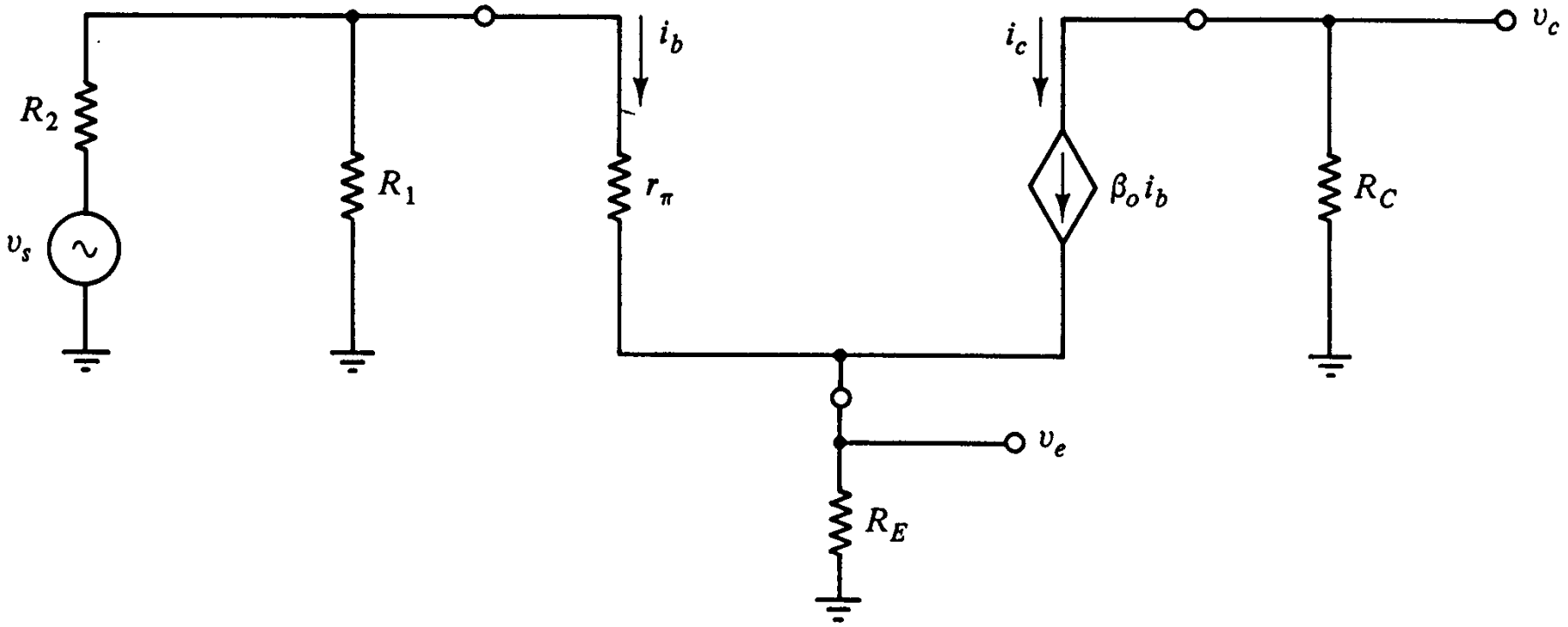


Figure 8.12
BJT in feedback bias configuration with input signal voltage source v_s.



(a)

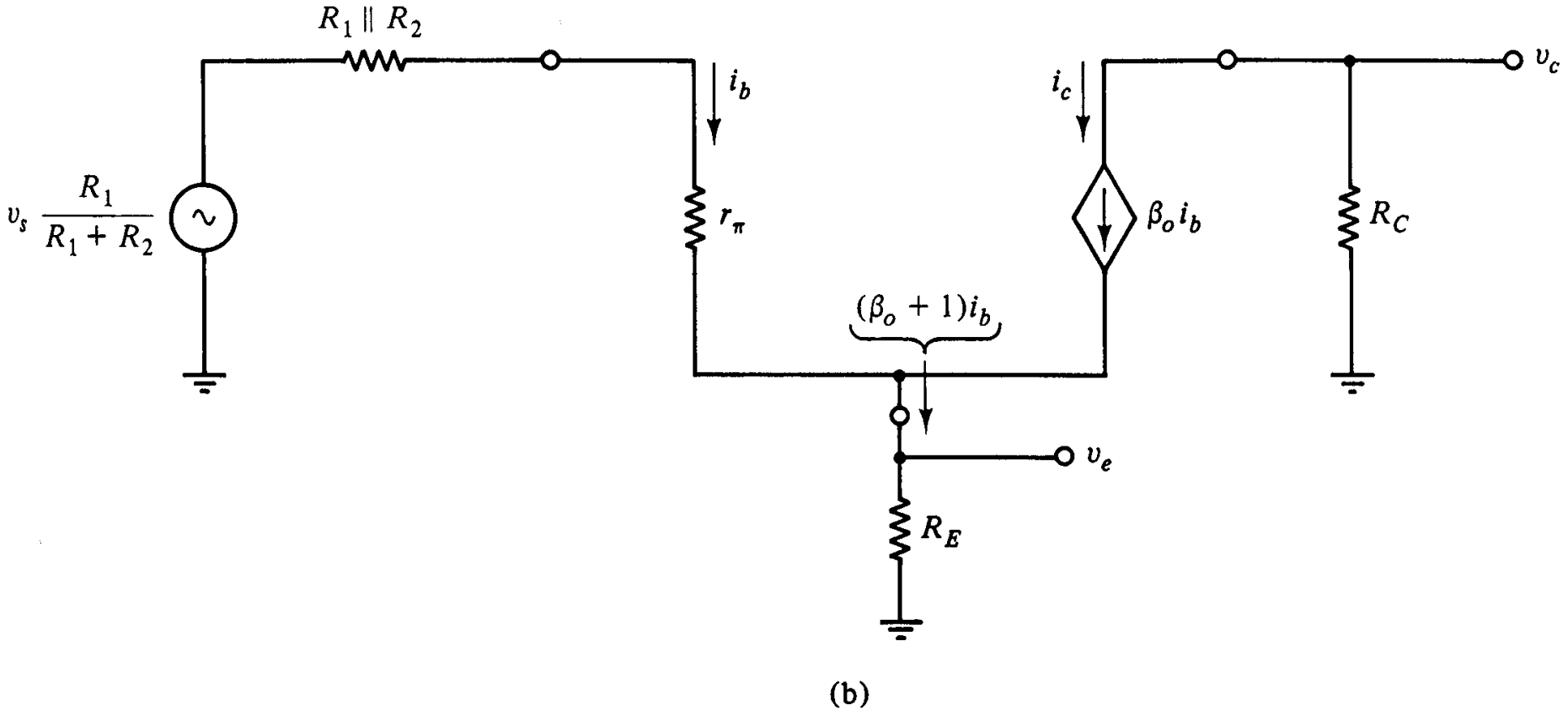


Figure 8.13 (a) Incremental model of the circuit of Fig. 8.12; (b) Thévenin equivalent used to represent v_s, R_1, and R_2.

Note: v_s connection does not represent typical amplifier design.

KVL around the input loop for incremental signal

$$v_s \frac{R_1}{R_1 + R_2} = i_b (R_1 \| R_2) + i_b r_\pi + (\beta_o + 1) i_b R_E$$

$$i_b = \frac{v_s \left[R_1 \middle/ (R_1 + R_2) \right]}{(R_1 \| R_2) + r_\pi + (\beta_o + 1) R_E}$$

$$v_e = (\beta_o + 1) i_b R_E = \frac{(\beta_o + 1) R_E \left[R_1 \middle/ (R_1 + R_2) \right] v_s}{(R_1 \| R_2) + r_\pi + (\beta_o + 1) R_E}$$

$$v_c = -(\beta_o i_b) R_C = -\frac{\beta_o R_C \left[R_1 \middle/ (R_1 + R_2) \right] v_s}{(R_1 \| R_2) + r_\pi + (\beta_o + 1) R_E}$$

In the limit $R_1 \| R_2 << (\beta_o + 1) R_E$

$\beta_o + 1 \cong \beta_o$

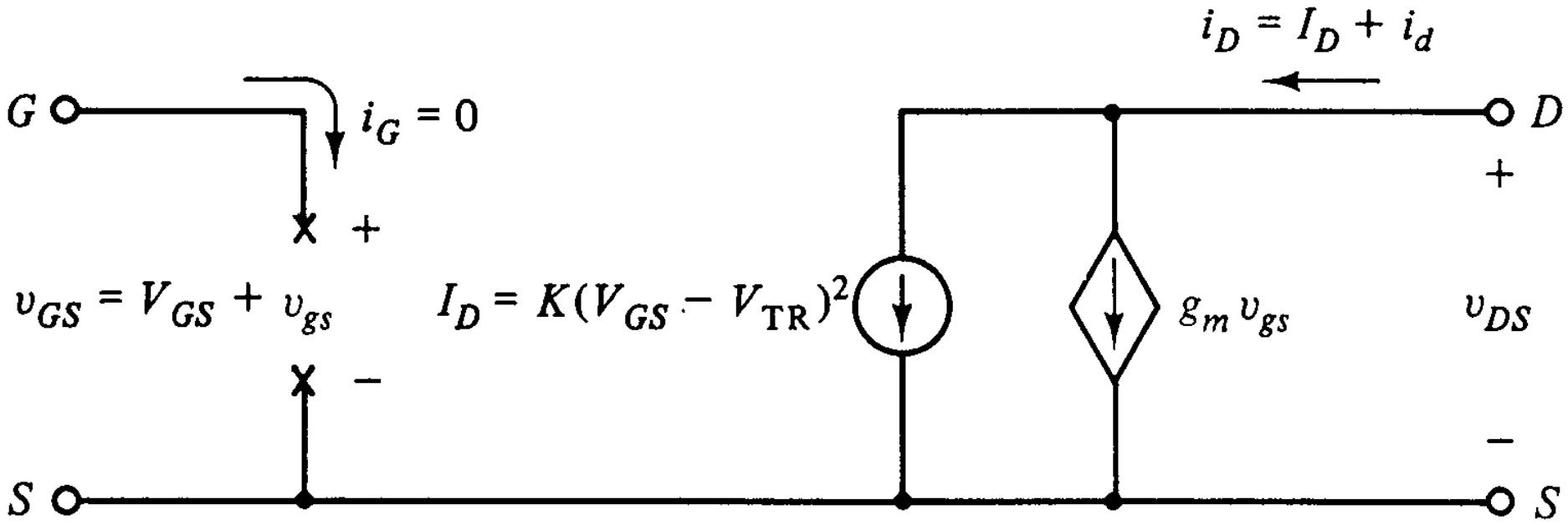
$r_p << (\beta_o + 1) R_E$

$$v_e \cong \frac{R_1}{R_1 + R_2} v_s$$

$$v_c \cong -\frac{R_C}{R_E} \frac{R_1}{R_1 + R_2} v_s$$

Incremental Model of MOSFET

Figure 8.14
Piecewise linear model for the input and output ports of an FET in the constant-current region. The value of I_D is determined by the bias value of v_{GS}.



$$g_m = \left.\frac{\P\, i_D}{\P\, v_{GS}}\right|_{V_{GS}, I_D} = \frac{\P}{\P\, v_{GS}}\left[k(V_{GS} - V_{TR})^2\right]_{V_{GS}, I_D} = 2k(V_{GS} - V_{TR})$$

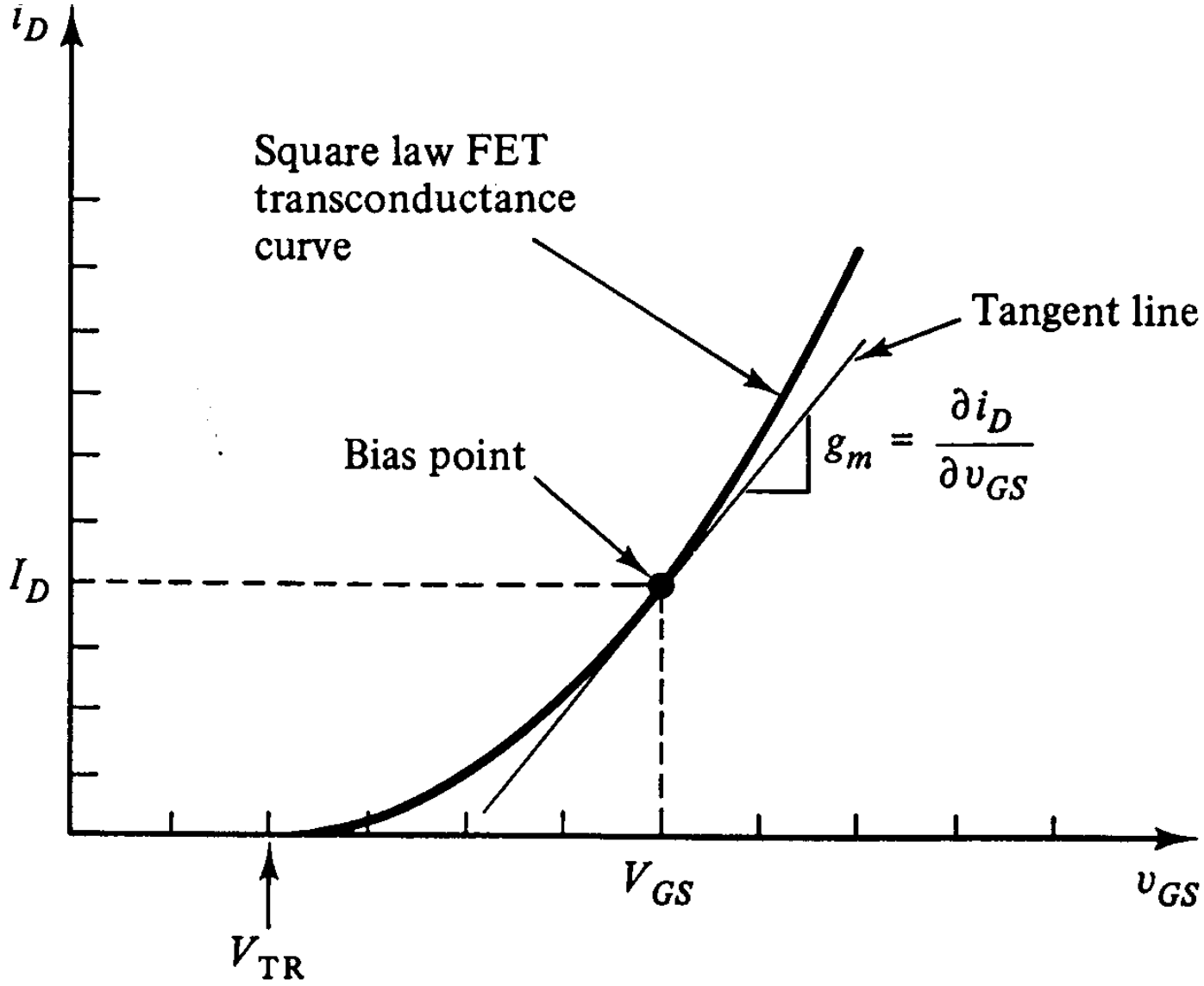
Assume constant current operation

$$V_{GS} - V_{TR} = \left(\frac{I_D}{k}\right)^{1/2}$$

$$g_m = 2\sqrt{k\, I_D}$$

Similar expression can be derived for JFET

Figure 8.15
FET transconductance curve and tangent line representing g_m.



- An incremental description for a FET can also be defined for triode (resistive) region
- It can be shown that the incremental model is as follows

Figure 8.24
For constant v_{DS}, incremental changes in v_{GS} cause changes in slope of the tangent to the v–i characteristic.

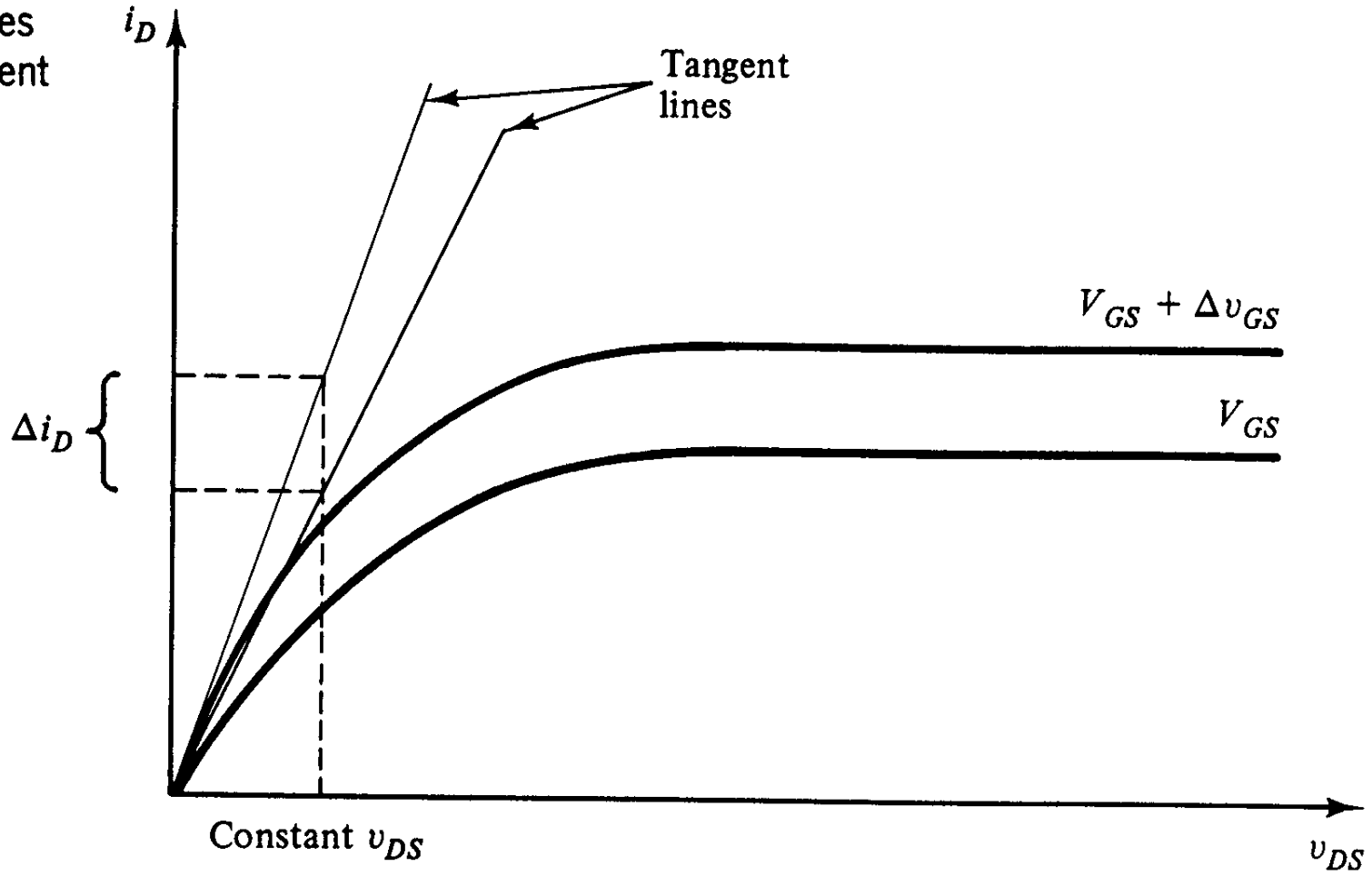
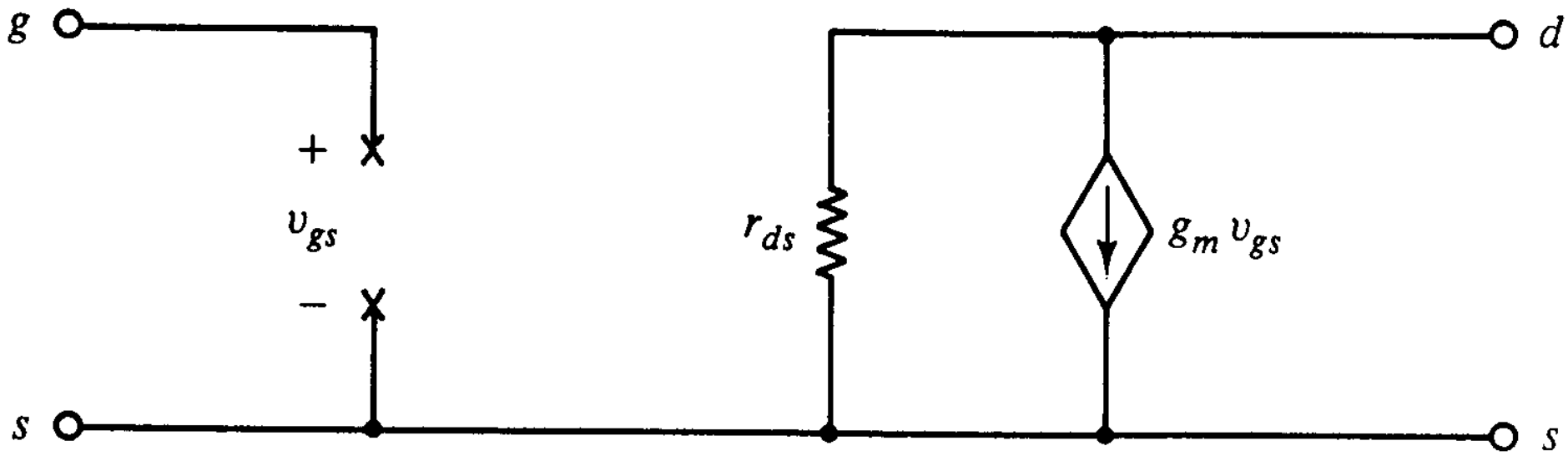


Figure 8.25
Piecewise linear model for a MOSFET in the triode region. This model contains no dc sources.



$$r_{ds} = \frac{1}{2k(V_{GS} - V_{TR})} \qquad g_m = 2k V_{DS}$$

Problem:

(A) Find the small signal componont of V_{OUT} for the following circuitd $v_s = 0.1$ Sin ωt, k = 0.2 mA/V^2, $V_{TR} = -2$ V.

(B) Find the Thevenin circuit between V_{OUT} and ground

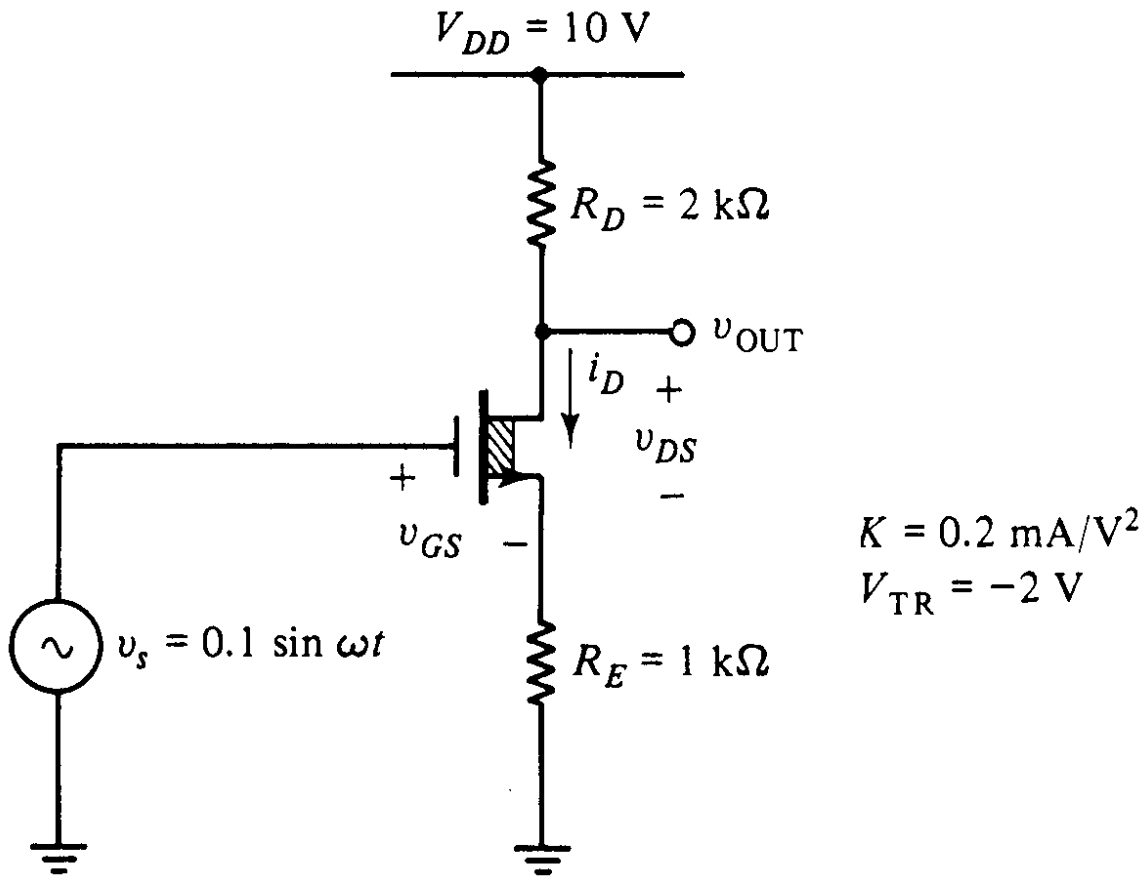


Figure 8.16
MOSFET inverter in feedback bias configuration.

The bias values can be found to be

$$I_D \cong 0.47\,\text{mA} \quad V_{GS} = -I_D R_E = -0.47\,\text{V}$$

Applying KVL to output loop

$$V_{DS} = V_{DD} - I_D(R_D + R_E) = 10\,\text{V} - (0.47\,\text{mA})(3\text{k}) = 8.6\,\text{V}$$

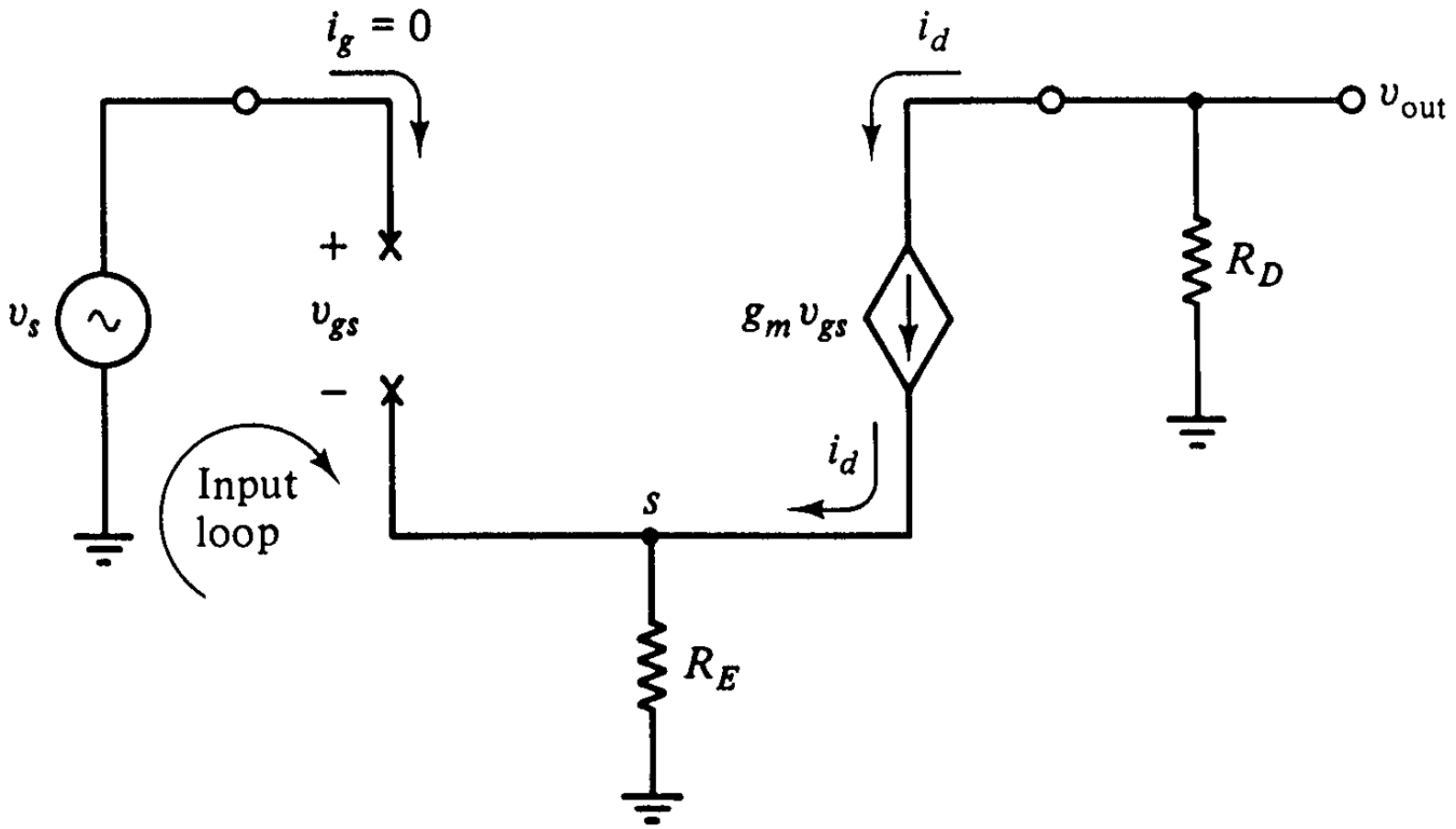
- Since $V_{DS} > (V_{GS} - V_{TR}) = 1.53$ V the device operates in the constant current region

The incremental transconductance g_m is given by

$$\begin{aligned} g_m &= 2k(V_{GS} - V_{TR}) \\ &= 2(0.2\,\text{mA/V}^2)\left[-0.47\,\text{V} - (-2\,\text{V})\right] \\ &\cong 0.61\,\text{mA/V} \end{aligned}$$

- The signal component of v_{OUT} can be found by substituting the PWL model and setting all DC sources to zero

Figure 8.17
Incremental model of the circuit of Fig. 8.16. All dc sources have been set to zero.



Applying KVL to the output loop

$$v_{gs} = v_s - i_d R_E = v_s - (g_m v_{gs}) R_E$$

$$v_{gs} = \frac{v_s}{1 + g_m R_E}$$

$\therefore$ Note feedback limits the fraction of v_s that appears as v_{gs}

$$v_{OUT} = -i_d R_D = -g_m v_{gs} R_D$$

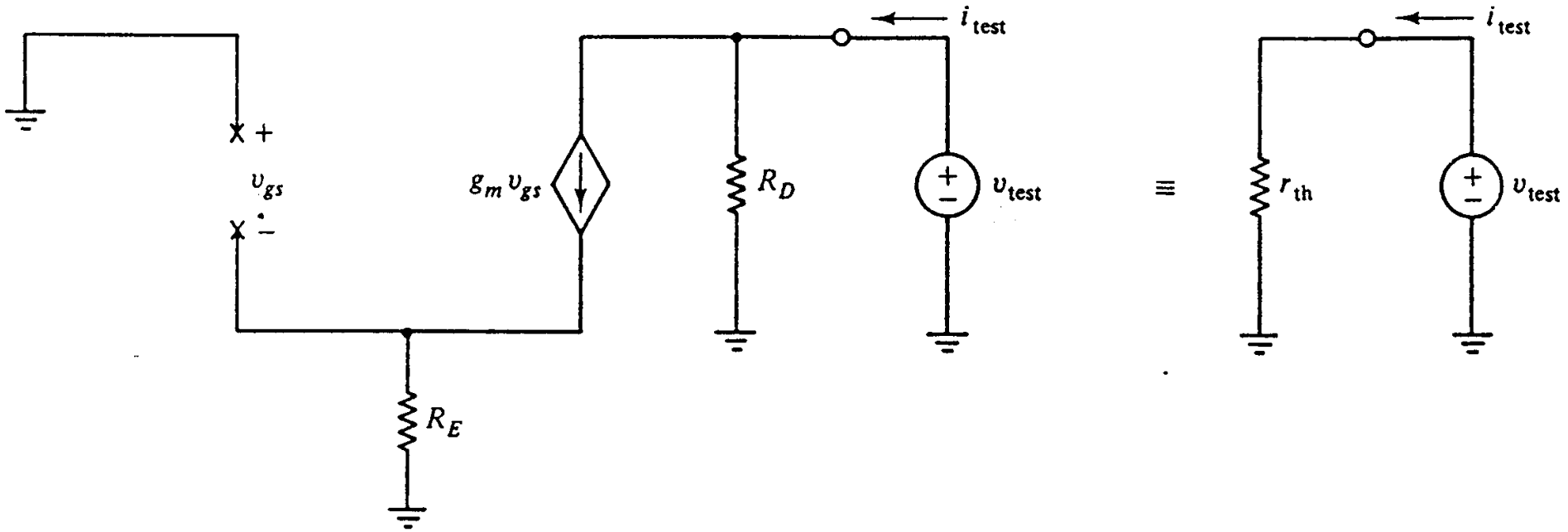
$$v_{OUT} = \frac{-g_m R_D}{1 + g_m R_E} v_s$$

$$a_V = \frac{v_{OUT}}{v_s} = \frac{-g_m R_D}{1 + g_m R_E} = \frac{-(0.61\,\text{mA/V})(2\,\text{k}\Omega)}{1 + (0.61\,\text{mA/V})(1\,\text{k}\Omega)} = -0.76$$

$$v_{OUT} = a_V v_s = (-0.76)(0.1 \sin \text{wt}) = -0.076 \sin \text{wt}$$

- Since v_{OUT} is computed with no load it represents the incremental open circuit Thevenin voltage
- The incremental r_{th} can be found by setting v_s to zero and applying v_{TEST}

Figure 8.18 Applying a test source to the output terminals of the incremental circuit of Fig. 8.18. The v_s source has been set to zero.



$$v_{gs} = g_m v_{gs} R_E \qquad \text{can only be satisfied if } v_{gs} = 0$$

$$i_{test} = \frac{v_{test}}{R_D}$$

$$r_{th} = \frac{v_{test}}{i_{test}} = R_D$$

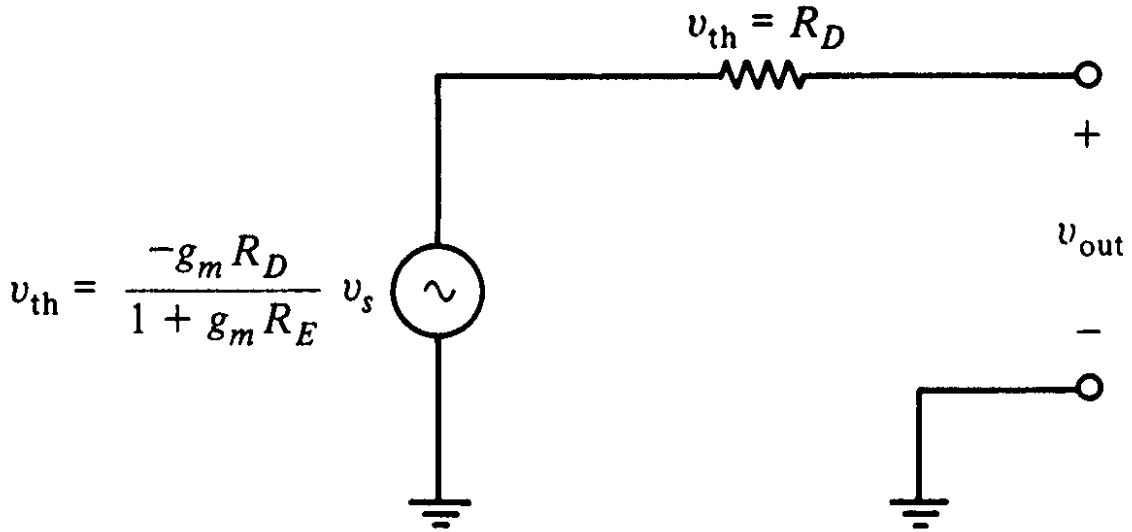


Figure 8.19 Incremental Thévenin equivalent of the circuit of Fig. 8.17 seen between the output terminal and ground.