ANN Based Modeling
of
High Speed IC Interconnects

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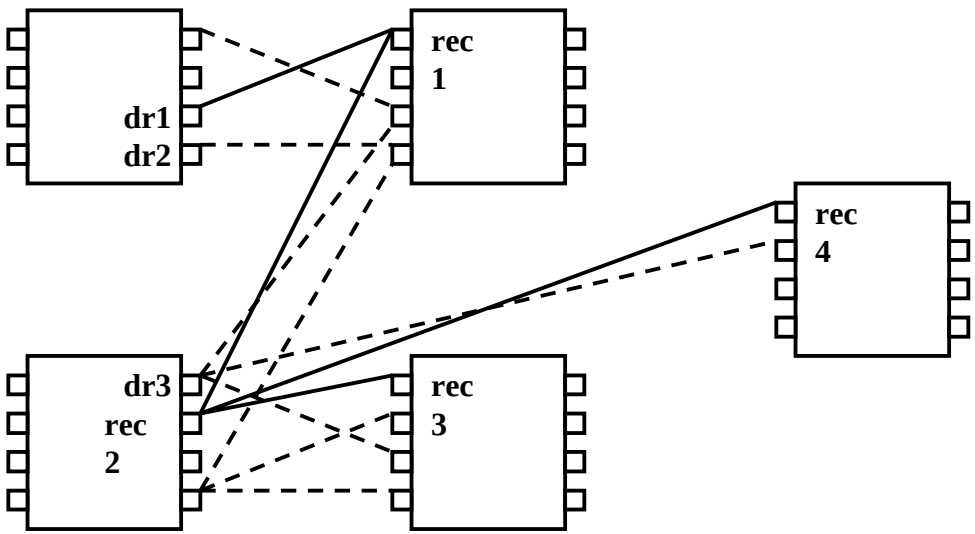
Needs for Repeated Simulation

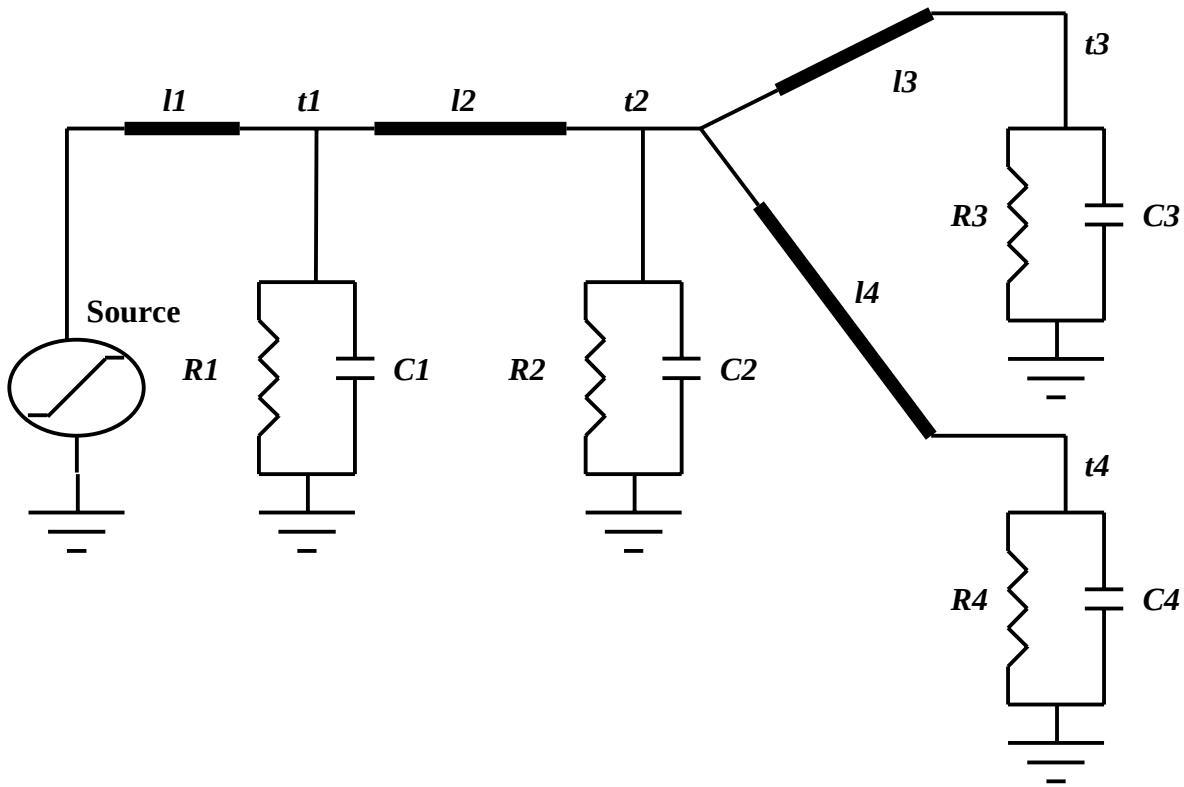
- **Signal integrity optimization**
- **Iterative design and re-optimization**
- **Monte-Carlo analysis**
- **Yield optimization**
- **Iterative design and yield re-optimization**

Applications and Numerical Examples:

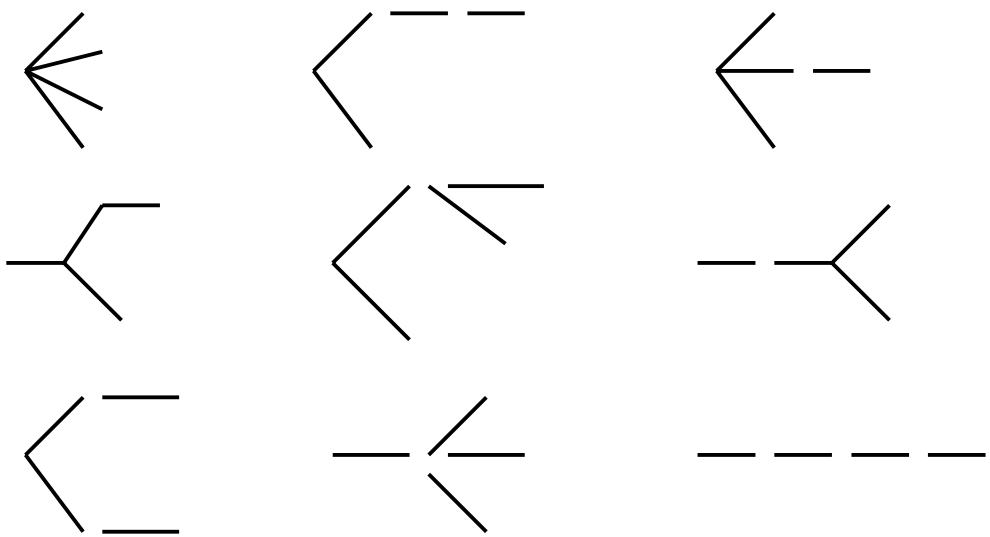
A typical interconnect network example (Veluswami, Zhang & Nakhla, 1995)



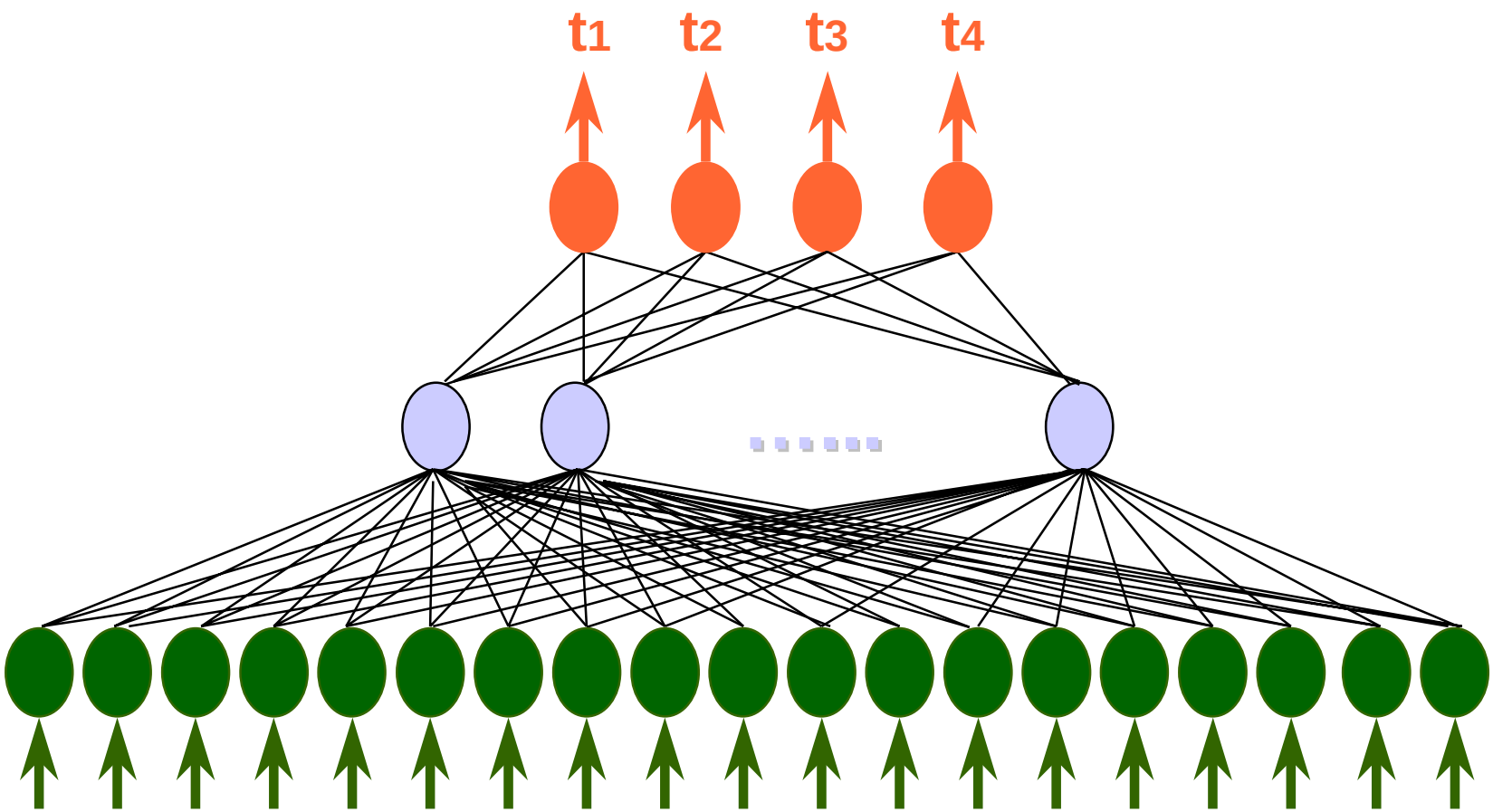
Electrical Equivalent of the Interconnect Configuration



Different Network Topologies for 4 Interconnects



Neural Network Model for 4 Interconnect Network



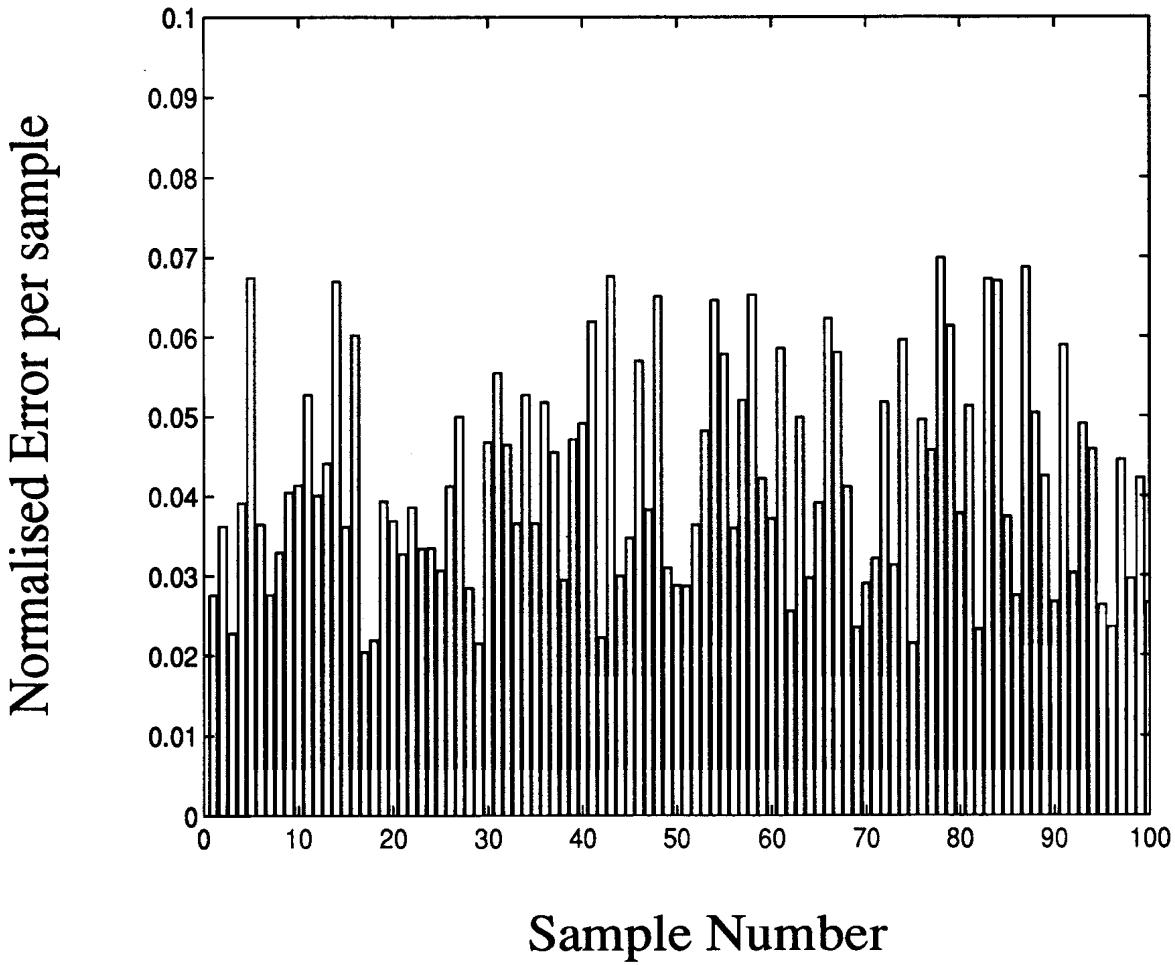
Input Variables and Their Range

Variable Name	Symbol	Range of Values
Interconnect Length	L_i	1 – 15 cm
Termination Resistance	*Ri*	100 – 100,000 Ohms
Termination Capacitance	*Ci*	3.3 – 5 nF
Source Resistance	*Rs*	13.3 – 45 Ohms
Input risetime	*Tr*	1.6 – 10 ns
Peak Voltage	*Vp*	0.8 – 5 V
Termination Vertices	*v*	2 – 6

CPU Time Needed for Simulation of 20,000 Circuit Configurations

Method	CPU time for delay
NILT	34.43 hours
AWE	9.56 hours
Neural Network	6.67 minutes

Normalised Error over 100 random Circuit Simulations

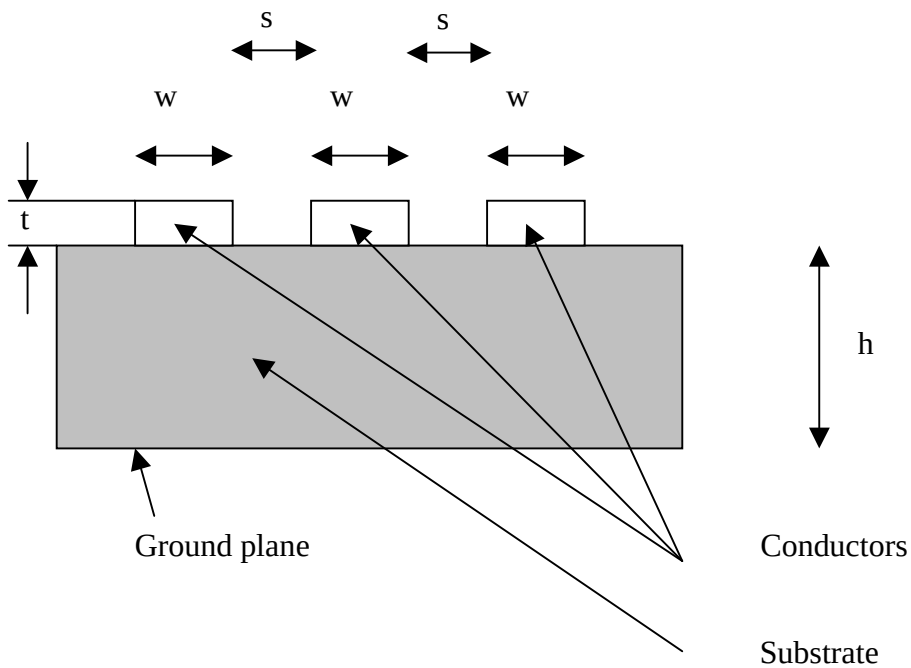


Performance Comparison for NILT, AWE and Neural Network Model:

	NILT	AWE	NNet
Number of configurations simulated per minute	9.69	34.88	3000
Factor of increase if Neural Network models are used	310	86	1

Three Parallel Coupled Interconnects

Cross-section of three parallel interconnects:



Neural Model:

Inputs: $x = [w, t, s, h, f]$

where

w – width of interconnects

t – thickness of interconnects

s – separation between conductors

h – height of substrate

f – frequency of operation

Outputs: The elements of the L and C matrices

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix} \qquad C = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix}$$

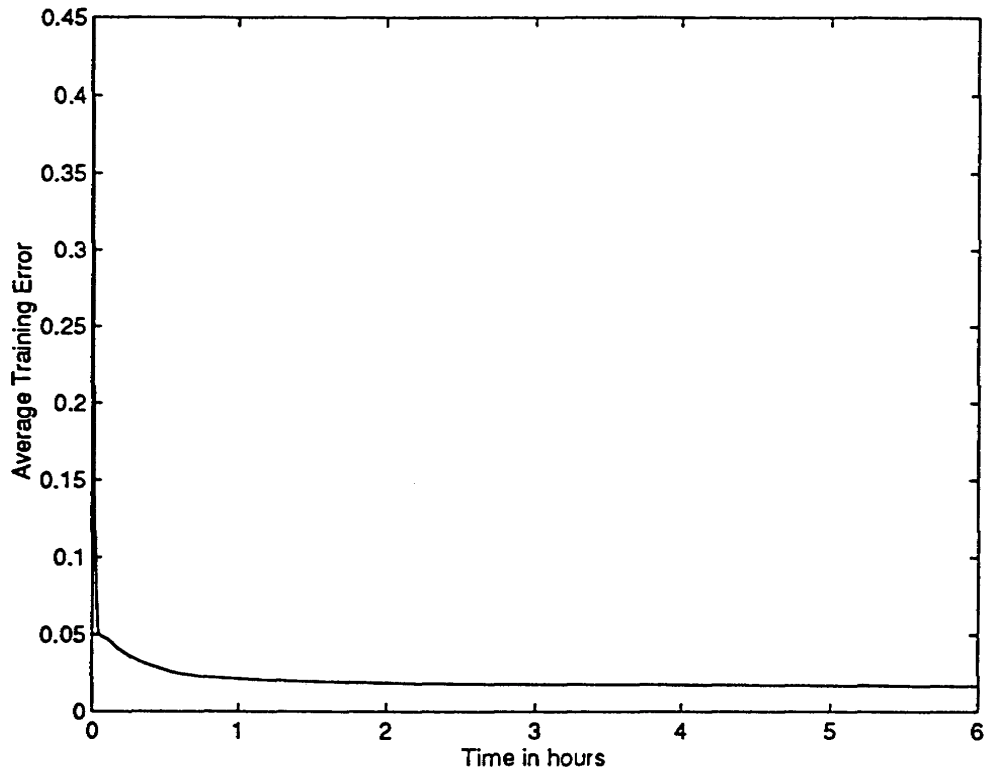
Neural Network Input Parameters and Their Range:

Parameter	Symbol	Minimum	Maximum
Conductor width	*w*	5 mil	11 mil
Conductor thickness	*t*	0.7 mil	2.8 mil
Separation	*s*	1 mil	16 mil
Substrate height	*h*	5 mil	10 mil
Frequency	*f*	1 MHz	8 GHz

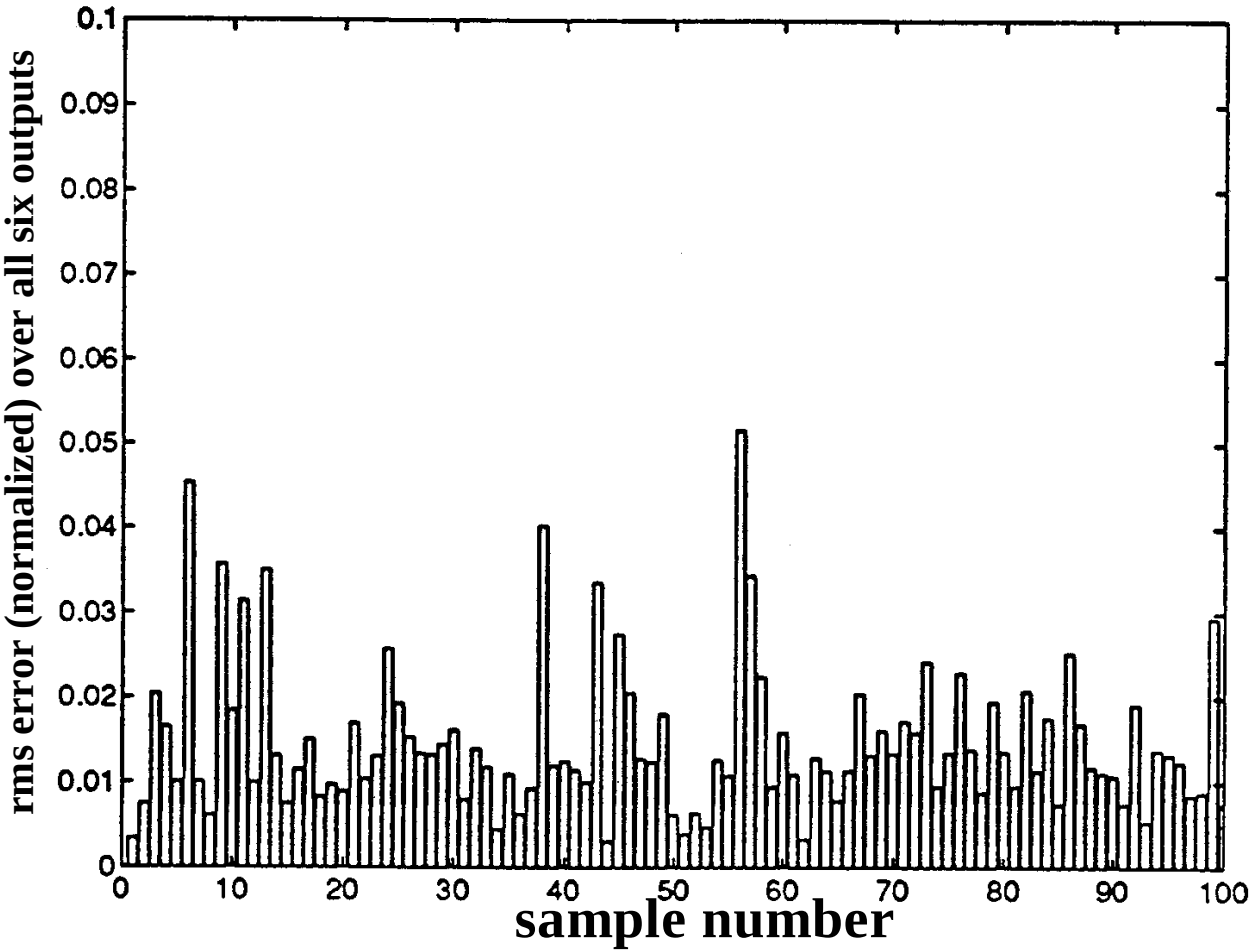
Features of Neural Network Model:

Feature	Value
Number of inputs	5
Number of outputs in the overall model	18
Number of output nodes in neural network	6
Number of neurons in the hidden layer	10
Size of model (in floating point numbers)	126
Size of training set	500
Size of test set	500
Data Generation Technique	SALI
Training time (in hours)	6
Average training error	0.0162
Average test error	0.0174

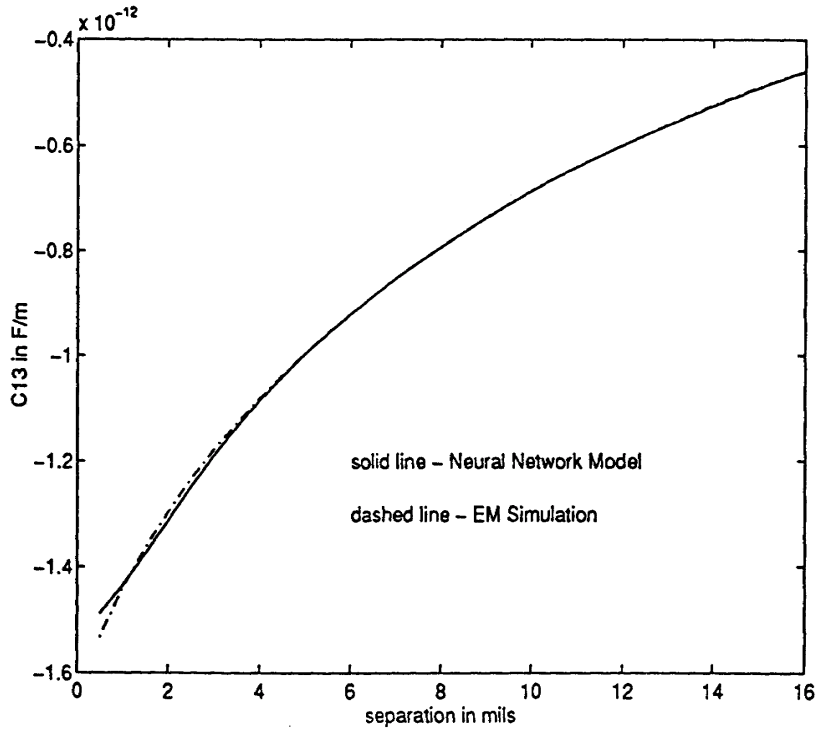
Average Training Error as Training Proceeded:



Test Error for 100 Random Inputs From the Test Set:

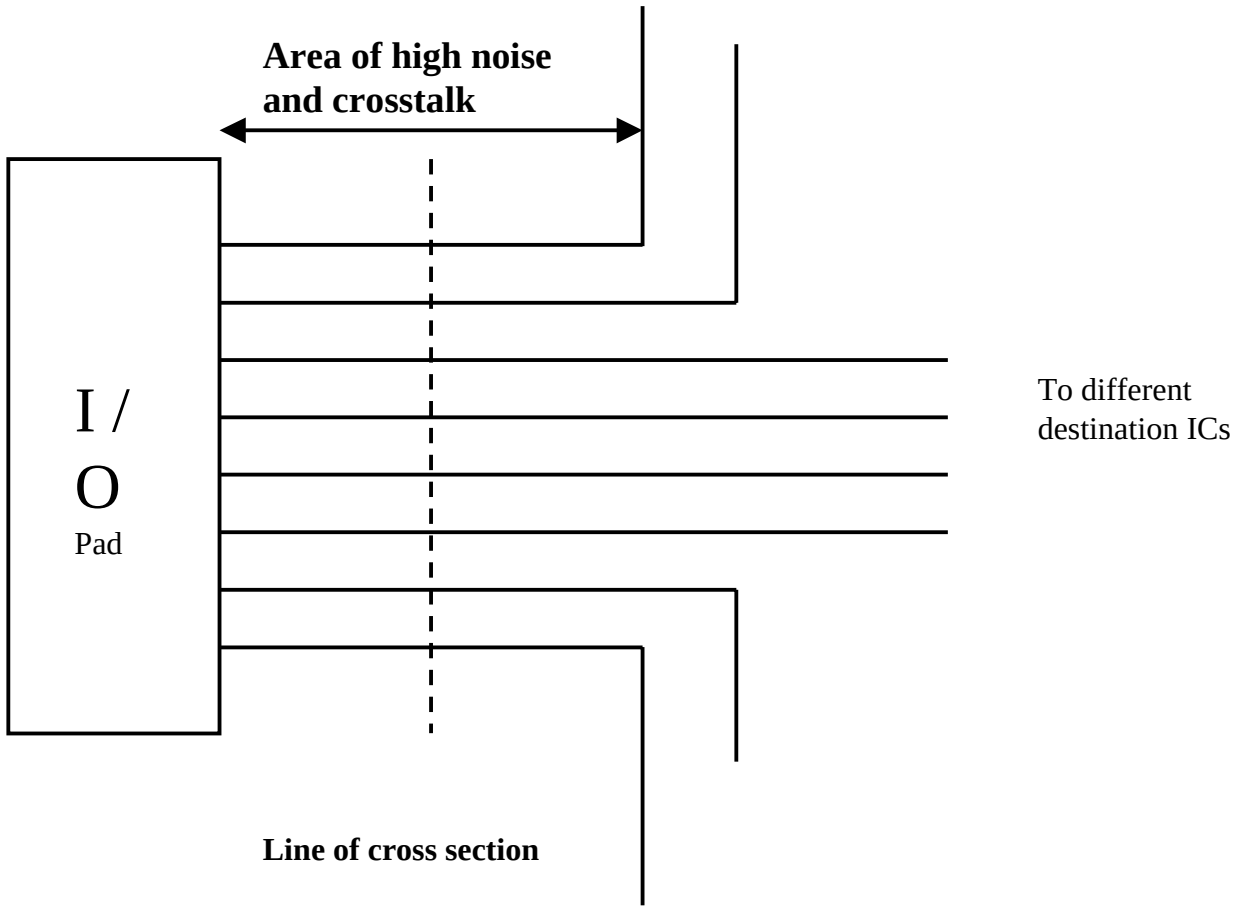


C_{13} as a Function of Separation, Keeping Other Parameters Constant:

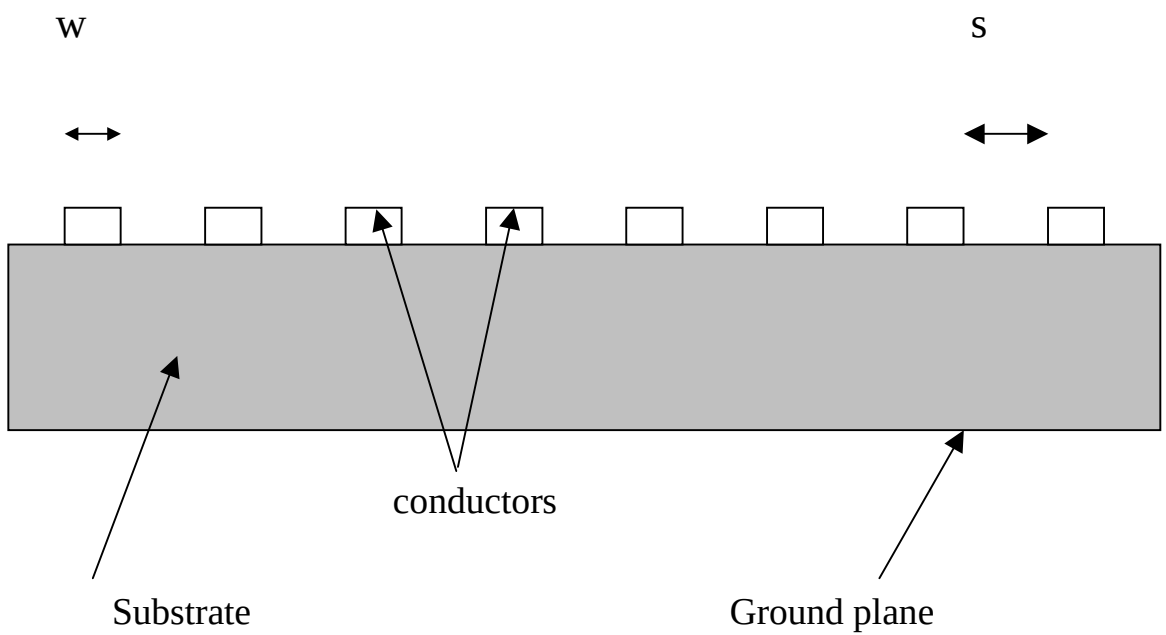


An 8-bit Digital Bus Configuration

8-bit bus on a PCB, showing region of high crosstalk and signal noise:



Cross-section of an 8-bit Digital Bus:



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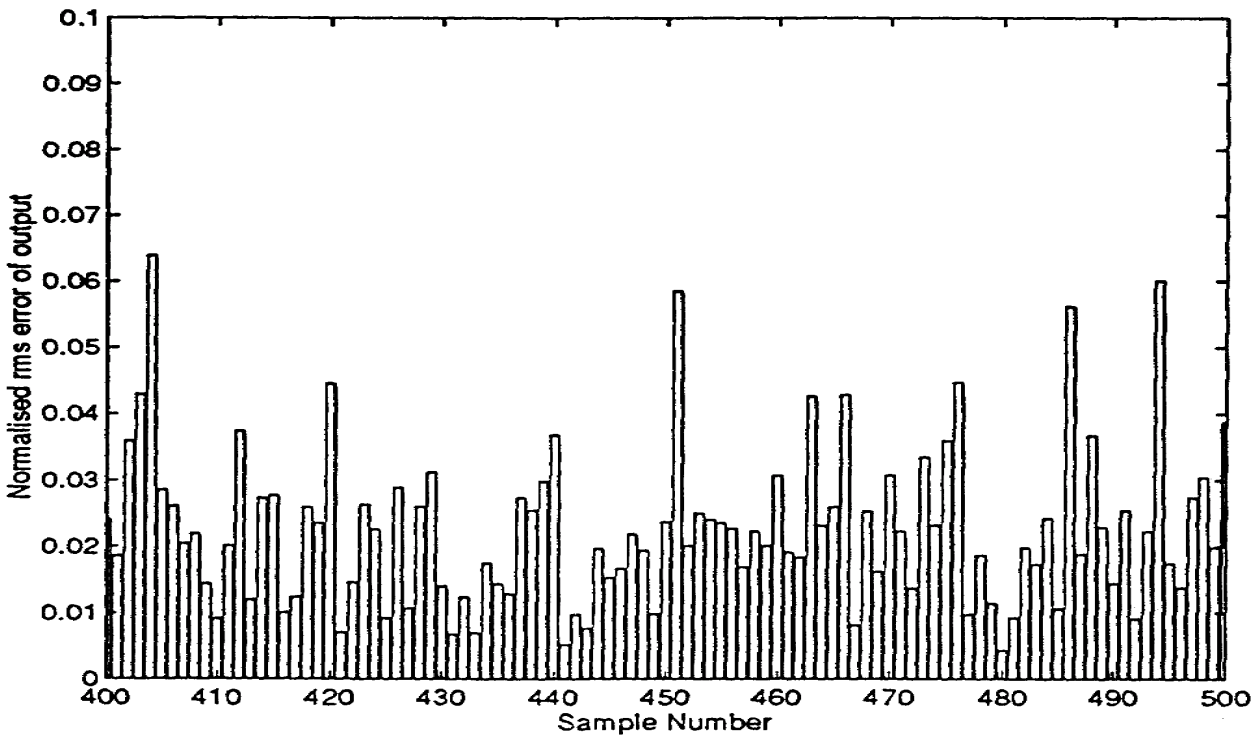
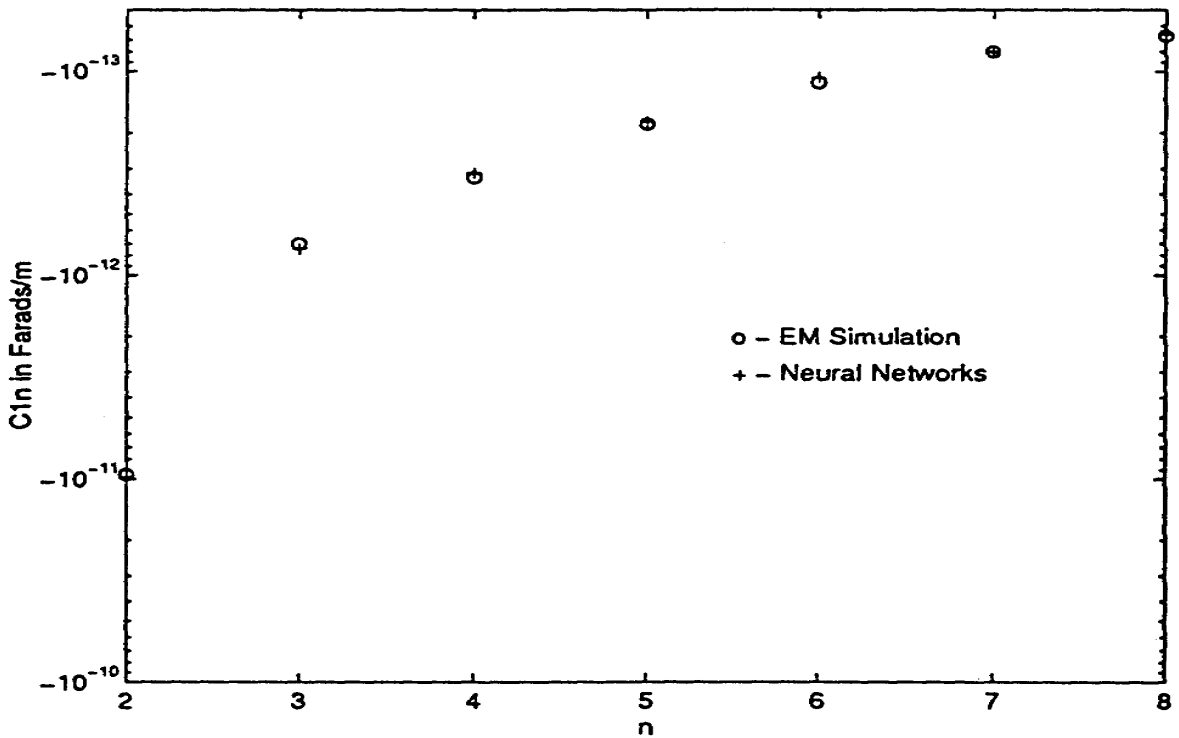
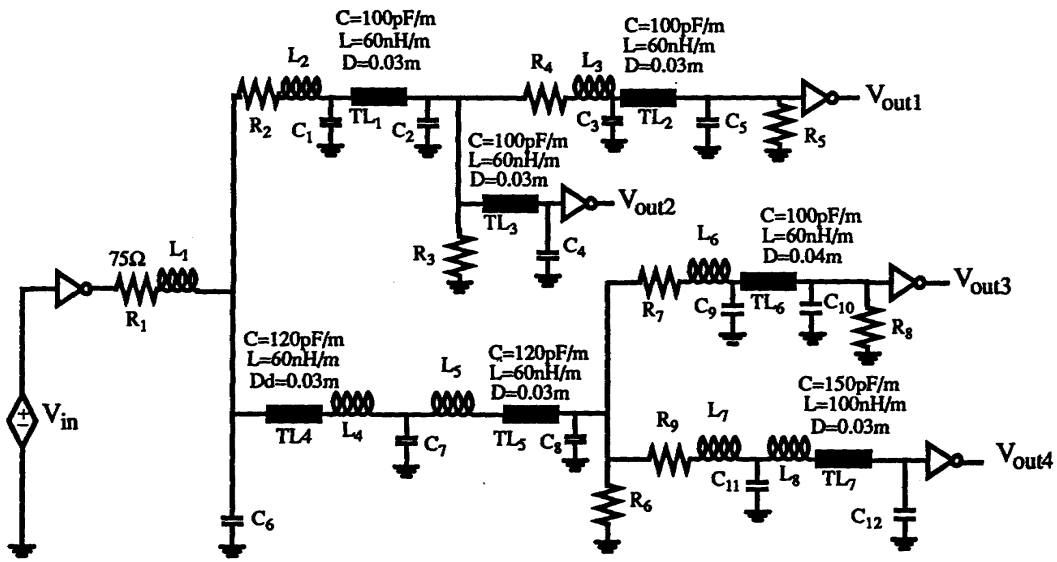


Mutual Capacitance:

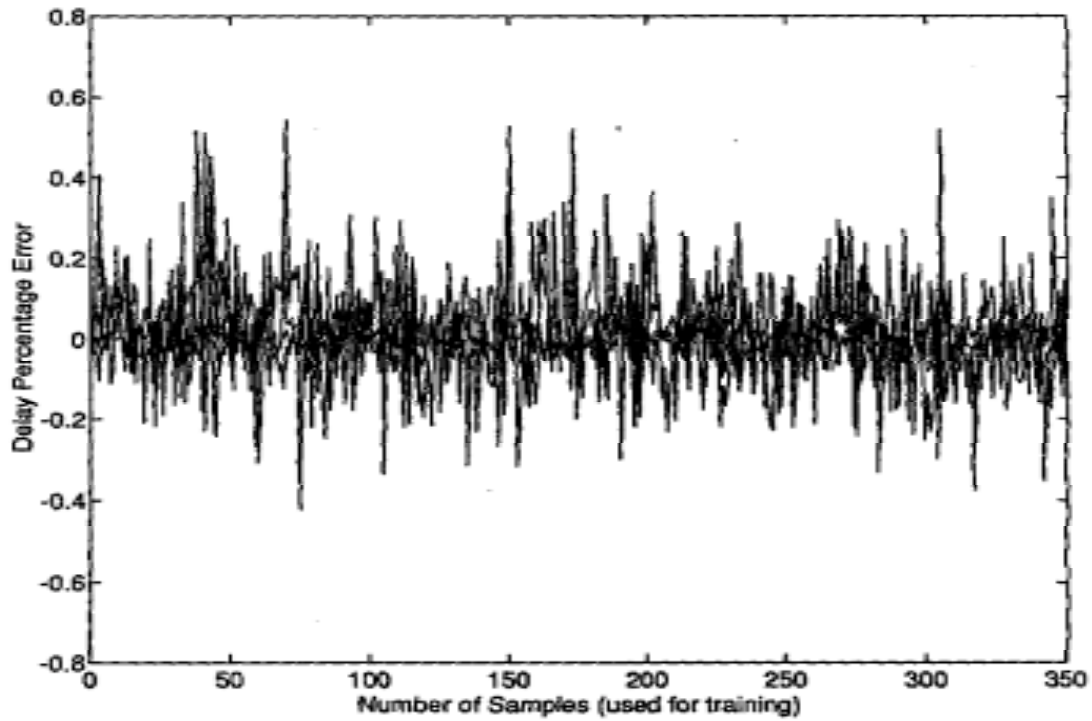


Transmission Line Circuit with Nonlinear Terminations (Zaabab, Zhang and Nakhla, 1995)

Use neural networks to model the response of a circuit. This figure represents a high-speed VLSI interconnect network modeled by 7 transmission lines and 5 nonlinear driver/receivers.



Signal delay through interconnect network is an important criteria in high-speed VLSI system design. The percentage error between the four delays predicted by the neural model and those obtained from Hspice for 350 training samples is shown as:



A comparison of the four integrity responses (delays of V_{out1} *through* V_{out4}) predicted by the neural network with those from Hspice was also made for 100 sets of randomly generated termination parameters not used for training. The result is shown as: