Lab 3: 741 Op-amp

Purpose:

The purpose of this laboratory is to become familiar with a two-stage operational amplifier (op-amp). Students will analyze the circuit manually and compare the results with SPICE. The op-amp in this lab is based on the 741 that you will study in class. Since the 741 is complicated, the opamp in this lab has been paired down to a more manageable size. Most notably the some bias circuitry has been made ideal and the output short circuit protection has been removed. This means that most, but not all of your simulation results will reasonably represent real-life behavior.

The 741 op-amp was once the work horse of circuit engineers due to its good performance (at audio frequencies) and low cost. As inevitably happens with all technology, newer chips improve on those in the past, and as a result, there are many op-amps available today that are faster, cheaper, smaller, less noisy, and more efficient, not to mention the fact that digital signal processing is gradually taking on the roles that traditional op-amp filters used to take. Still, the 741 is relatively easy to analyze, and shows all of the important aspects of an op-amp. Its limitations are actually useful for as since we can measure them easily using relatively cheap lab equipment and simple simulation software.

Introduction:

Before proceeding with the laboratory, students are advised to read Sedra and Smith, "Micro-Electronic Circuits", the section in Chapter 10 on the 741 op-amp.

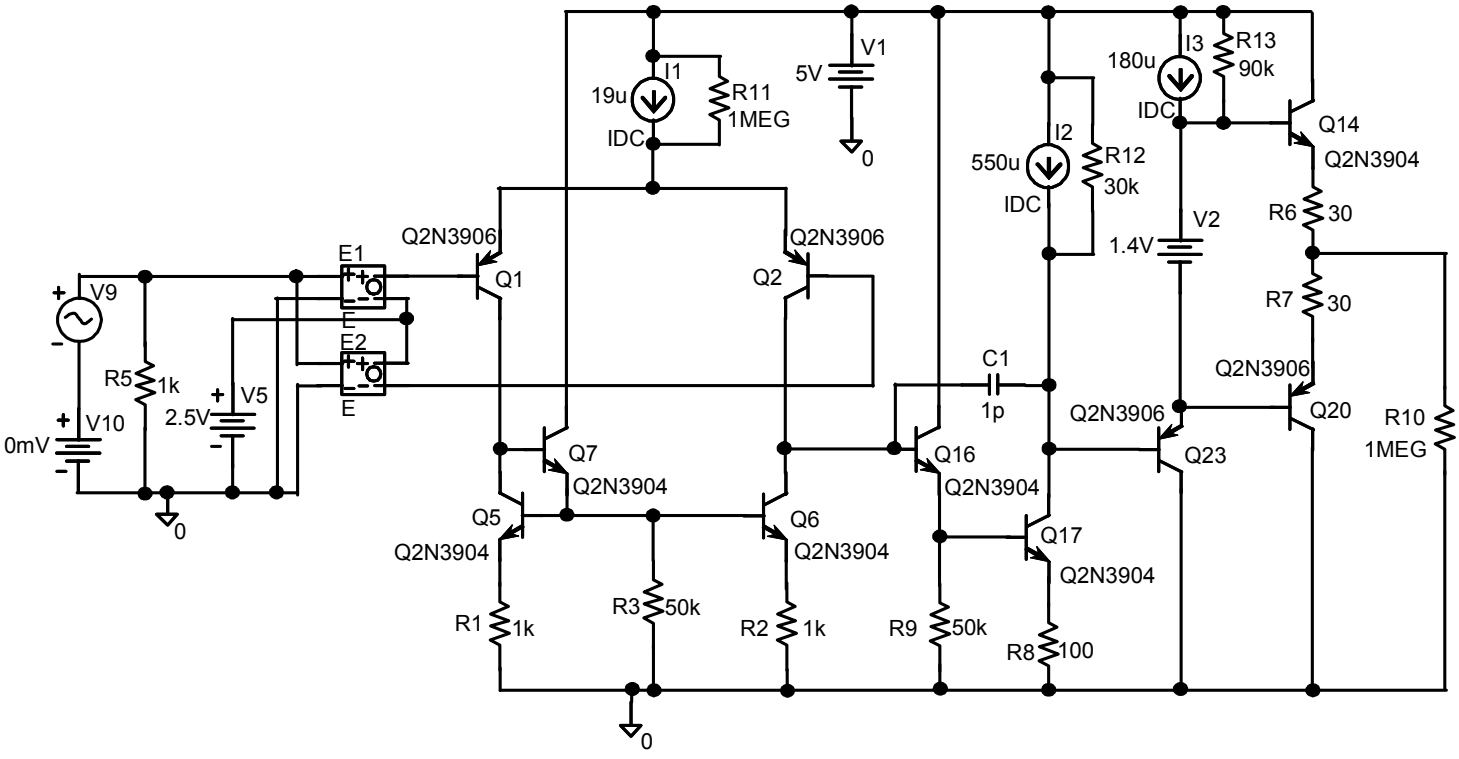


Figure 3.1 A scaled-down 741 op amp used in this lab

Figure 3.1 shows the op-amp circuit that you will be simulating using SPICE. The base of Q_2 is the non-inverting input and the base of Q_1 is the inverting input of the op amp. V_{10} is the input

DC voltage, which can be used to represent input offset voltage, or be used for input DC voltage sweeps. V_9 is the input sinusoidal voltage, which can be used for AC analysis. The boxes labeled E1 and E2 are voltage-controlled voltage sources each with a gain of ½. This allows the input voltage (the sum of V_9 and V_{10}) to be applied differentially to the two inputs, while adding the common-mode voltage V_5 to each input.

Prelab:
Using the following assumptions for NPN and PNP parameters, calculate the following (there are sample calculations at the end of the lab to give you a starting point). This must be done by the first day.

Parameter	**NPN**	**PNP**
Early Voltage V_A	80 V	20 V
Beta (assume constant but note that it normally depends on current)	100	100
I_S (recall that $I_C = I_S e^{\frac{V_{BE}}{V_T}}$)	6.73 fA	1.41 fA
VBE	0.6 V	0.6 V
VCC	5 V	

For each calculation, make sure to show the small signal equivalent circuit you are using. Your work should be complete without referencing the textbook or notes for figures or equations. Note that all of this work needs tobe integrated in your report.

- I_c, r_o and g_m, for every transistor, in addition to the function of each transistor. You can assume that V_A (the early voltage) is 80V for the NPN transistors and 20V for the PNP transistors. Note that the transistor output resistance r_o is approximately given by V_A/I_C. You may assume that β=100 for all transistors, (although in reality, β is not constant but depends on the current). Put the results in a table and show all calculations.
- The gain of the first stage A_1. This means the gain from the input to the base of Q_{16}, including the impedance seen looking into the base of Q_{16} as a load to the first stage.
- The gain of the second stage A_2. This means the gain from the base of Q_{16} to the base of Q_{23}.
- The gain of the third stage A_3, as measured from the base of Q_{23} to the output across R10. Note that this gain will be much smaller than the other 2. Note that you cannot just simply assume the gain is 1- even if it is a common collector circuit, you must go through all the steps.
- The common mode gain of the first stage and of the entire op-amp.
- The common mode rejection ratio
- The differential gain.
- The input common-mode range. Note that the circuit has a 5V supply.
- The output voltage swing.
- The value for the capacitor C_1, so that the unity-gain frequency f_u = 1 MHz. Note that this will NOT be 30pF as specified in S&S.
- The slew rate of the op amp. Note that this will be limited by how fast the input stage can charge or discharge the capacitor C_1.

Answer all of the following questions:

- Explain the difference in role of V_{10} and V_5. Why are both needed?

- What is the purpose of Q_7 and R_3 in this circuit? What difference would there be if instead of both, the collector and base of Q_5 were shorted as in the current mirror in Lab 1? You may want to consider the impact of Q_{16}.
- What is the role of C_1 and what would happen if it were absent?
- The circuit uses ideal current sources. How would these be implemented in a real circuit? What differences in performance might be seen as a result? The answer is not finite output impedance since the output impedances are already modeled byR_{11}, R_{12} and R_{13}.
- What is the purpose of V_2? How would V_2 be implemented in a real circuit?
- Why are 3 stages used in this op-amp design? Why bother with the third stage if it provides such a low gain?
- What is the DC power consumption of the entire circuit (assume no input signal).

The calculations MUST be done before entering the laboratory. Failure to do so will result in the forfeiture of ALL pre-lab marks.

Experiment:
In day 1: Do at least Part 1. In Day 2, do Part 2 and 3. It is possible to do all 3 parts in 1 day- if you do so, you do not need to come back for the second day. There is no pre-lab for day 2.

You should load up the schematic for Figure 1, provided by the TAs. For C_1, use the value calculated in the pre-lab. Figure 1 also shows the input source arrangements that should be used for differential and common mode signals.

Part 1
Perform the following tasks and answer all questions:

1. Do a DC sweep of the input differential voltage V_d between -10 mV to 10mV, while the common mode voltage V_{cm} is set to 2.5 V. Plot the transfer curve for V_o versus V_d.
   From the plot, what is the range of the linear region (the range for which the output is a linear multiple of the input)? What is the output voltage swing? Estimate the differential gain. What is the input offset voltage (*i.e.*, the value of V_d required for the output to be 2.5V)? Compare the values obtained by SPICE to the ones calculated. If the values differ, explain why.
   In your report, compare these values with the values you calculated in your pre-lab. Refer to each number separately and do not be vague. Explain any differences.

2. When you did the calculations in the pre-lab you used approximate values for the transistor parameters (I_C, g_m, r_o, β, etc.). You can get the actual values for all these parameters from the SPICE DC simulation that you just ran in step one (make sure you have asked for bias point detail in analysis setup, then after the simulation click on analysis and examine output).
   Print out these values and include them with your lab report in the appendix. In your report, insert a table showing side-by-side comparisons of your calculated values against the simulated values. Explain any discrepancies and explain whether or not they are significant.
   Redo your calculations using these numbers and recalculate the differential gain. Compare it with the one calculated previously. If the values differ, explain why. Show a table in your report listing side-by-side comparisons of the original gains and the

recalculated gains. Which calculations have the smaller error? Why? What can you conclude about the accuracy of the equation you used to calculate the gain?

3. Do a DC sweep of the common-mode voltage from 0V to 5V, while the differential voltage V_d is set to the input offset voltage. Plot V_o versus V_{cm} transfer curve. What is the common-mode range? What are the common mode gain and the common mode rejection ratio? Compare all of these values to the ones calculated in the pre-lab. If the values differ, explain why.

Part 3

Frequency Response

The frequency domain of the circuit is examined in this section. You will use the circuit configuration shown in Figure 1 for this part. Plot the differential magnitude and phase response of the circuit using SPICE between 1 Hz to 10 MHz with the input voltage set to unity. From the SPICE results, what is the unity gain frequency f_u? Compare this result with the value calculated in the pre-lab.

Part 2 Slew Rate

The slew-rate is the maximum rate-of-change of the output voltage. It is usually measured with the op amp in the unity-gain voltage-follower configuration. The circuit configuration is shown is Figure 2. The input voltage of Figure 2 is a square wave generator, stepping between 1V and 4V. The square wave has a period of 50us with a 0.1us rise and fall time. Plot the input and output transient voltage waveforms. From the SPICE plots, what is the positive and negative slew rate expressed in V/us? Compare the SPICE values with the slew rate calculated in your pre-lab.

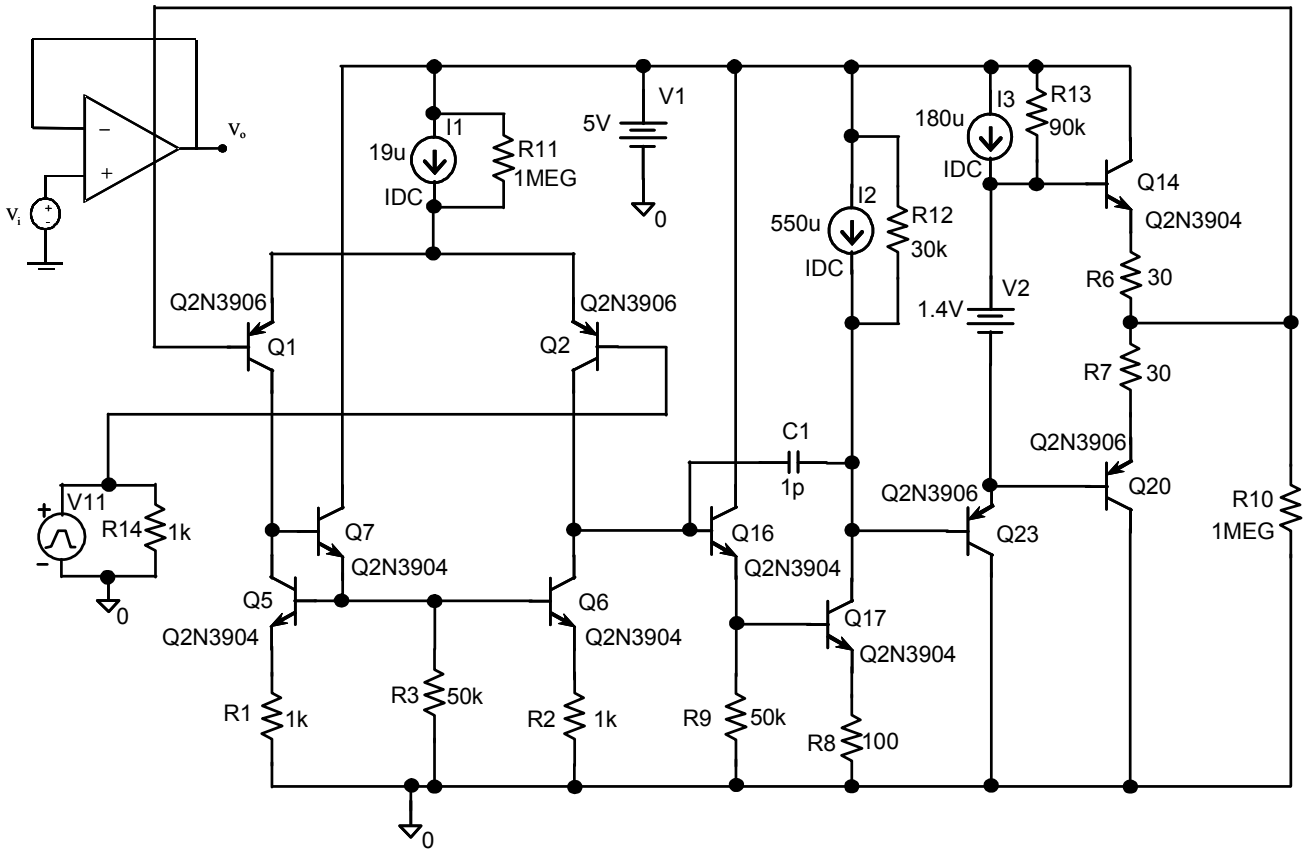


Figure 3.2 Opamp set up in unity gain mode for slew rate simulation.

Op Amp Sample Calculations

In the following pages are some handwritten notes on the analysis of the 741 opamp. This will give you some more information, but will not give you the full answer – that is for you to work out. For example, the effect of the resistors in parallel with current sources will be that the total current is higher than the current source value. This has not been included in these sample calculations (except once just before the first schematic and it has a line through it when we decided to stick with the simple estimate of current).

In order to give you a starting point, the following set of calculations calculates some of the properties of an op-amp. Note that there are some differences in the circuit, in order to give you the incentive of actually doing the work yourself. Also note that there are some errors in the calculations- these have been left in deliberately as an exercise for the student.

The following schematic has been used. This is a reminder that this is a modified version of the 741 Op-Amp that you are to use. DO NOT COPY THESE NUMBERS.

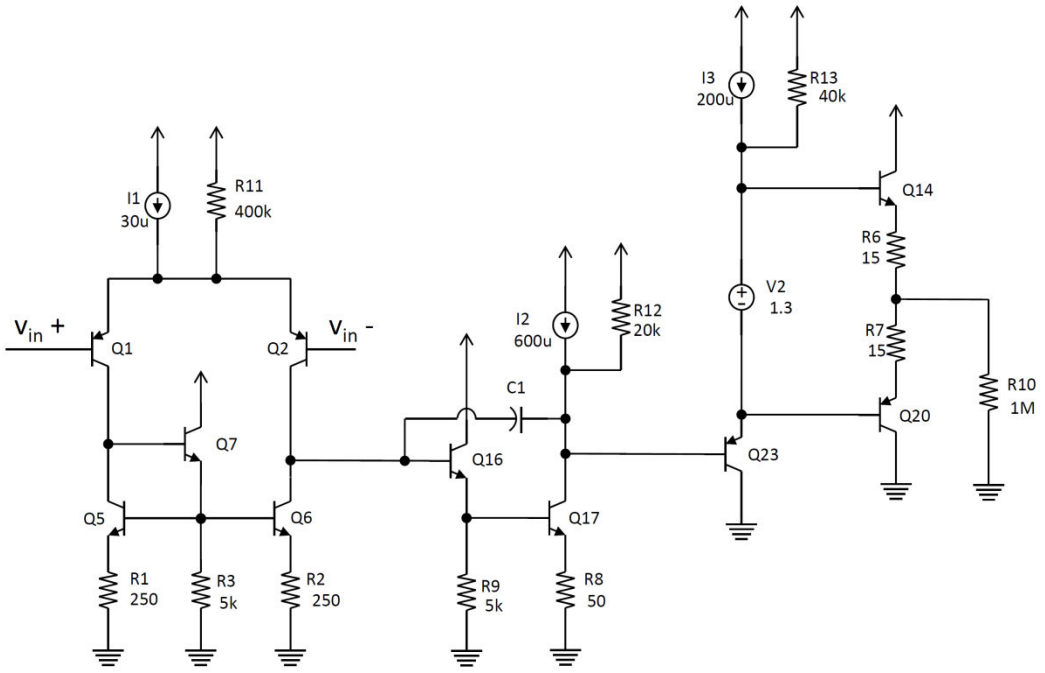


Figure 3.3 Schematic of op-amp used for sample calculations. Note that nearly all component parameters have been changed

The following parameters are being used:

Parameter	**NPN**	**PNP**
Early Voltage V_A	30 V	10 V
Beta (assume constant but note that it normally depends on current)	200	200
I_S (recall that $I_C = I_S e^{\frac{V_{BE}}{V_T}}$)	12.5 fA	7.5 fA
V_{BE}	0.5V	0.5V
V_{CC}	3.3V	

First, let us assume that the output is half of V_{CC}, and so is 1.65 V. Then, we can solve for the current flowing through Q_{14} and Q_{20} (ignore the load current for now).

Note that we cannot just assume a V_{BE} of 0.5 V for these transistors because the current flowing through this line is strongly affected by the V_{BE} of Q_{14} and Q_{20}. For the other transistors, we can make this assumption because the design of the circuit makes the bias point less dependent on the transistor parameters. We will investigate the impact of this sensitivity on the op-amp performance later.

Around the output, we can create the following loop equation:

$$1.3 = V_{BE20} + R_7 I_{E20} + R_6(I_{E20} + I_{R10}) + V_{BE14}$$

Remember that

$$V_{BE} = V_T \ln \frac{I_C}{I_s}$$

$$1.3 = V_T \ln \frac{I_{C20}}{I_{s20}} + R_7 I_{E20} + R_6(I_{E20} + I_{R10}) + V_T \ln \frac{I_{C14}}{I_{s14}}$$

And since that

$$I_C = \frac{\beta}{\beta+1} I_E$$

$$1.3 = V_T \ln \frac{\frac{\beta_{20}}{\beta_{20}+1} I_{E20}}{I_{s20}} + R_7 I_{E20} + R_6 (I_{E20} + I_{R10}) + V_T \ln \frac{\frac{\beta_{14}}{\beta_{14}+1} (I_{E20} + I_{R10})}{I_{s14}}$$

$$1.3 = 0.025 \ln \frac{\frac{200}{201} I_{E20}}{7.5 \times 10^{-15}} + 15 I_{E20} + 15 I_{E20} + 0.025 \ln \frac{\frac{200}{201} I_{E20}}{12.5 \times 10^{-15}}$$

$$1.3 = 0.025 \ln(1.3267 \times 10^{14} I_{E20}) + 30 I_{E20} + 0.025 \ln(0.796 \times 10^{14} I_{E20})$$

$$1.3 = 0.81297 + 0.025 \ln(I_{E20}) + 30 I_{E20} + 0.8002 + 0.025 \ln(I_{E20})$$

$$0 = 0.3132 + 20 I_{E20} + 0.05 \ln(I_{E20})$$

Solving numerically gives $I_{E20} = 1.19\text{mA}$. This then lets us calculate the node voltages and currents the normal way. Note that this value of current is much larger than the current flowing through R_{10}, making our assumption of ignoring it valid. If the current was much smaller, we would need to redo our calculations.

Using the calculated currents, the BE voltages for Q_{14} and Q_{20} can be found.

$$V_{BE20} = V_T \ln \frac{I_{C20}}{I_{s20}} = 0.025 \ln \frac{1.18 \times 10^{-3}}{12.5 \times 10^{-15}} = 0.6318V$$

$$V_{BE14} = V_T \ln \frac{I_{C14}}{I_{s14}} = 0.025 \ln \frac{1.18 \times 10^{-3}}{7.5 \times 10^{-15}} = 0.6445V$$

This can be used to get the node voltages for the last state (note some rounding was done- high precision is not really required here due to all of the approximations we are making).

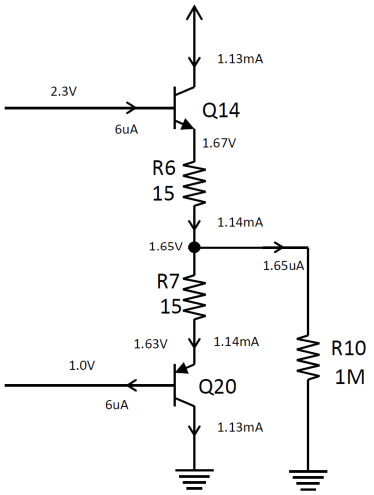


Figure 3.4 Schematic of last stage showing node voltages and line currents

The next step is to determine the current flowing through Q23. Since we know the node voltages for V2, we can calculate the current flowing through R13.

$$I_{R13} = \frac{V_{CC} - V_{2+}}{R_{13}} = \frac{3.3 - 2.3}{40000} = 25uA$$

Combined with the current source and the 2 base currents of Q14 and Q20, we get a collector current of 225 uA, and we can calculate the remaining currents. We also assume that the BE junction voltage is 0.5 V

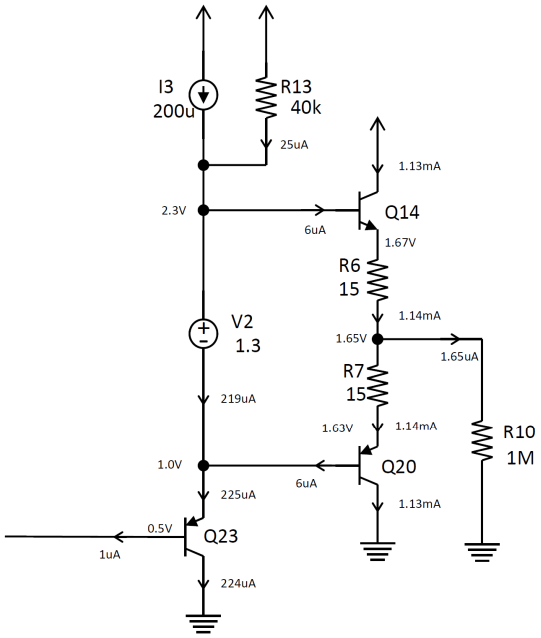


Figure 3.5 Schematic of last stage and Q23, showing node voltages and line currents

Similarly, we then calculate the current flowing through R12, and then find the total current flowing through the Q17. The emitter current flows through R8, allowing use to get the emitter voltage, and by extension, the base voltage (using VBE=0.5 V).

This, in turn lets us calculate the current flowing through R9, and then we can get the node voltages and currents for Q16.

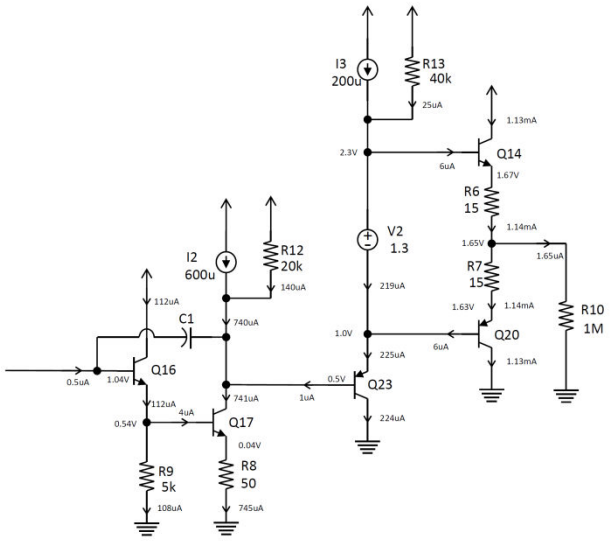


Figure 3.6 Schematic of second two stages showing node voltages and line currents

This leaves us with the input stage. First, we recall that the input common mode voltage is 1.65 V, and we assume each BE junction is 0.5V. This gives us the shared emitter voltage, and the current flowing through R11. Then, we can fill out the rest of the circuit.

Looking at the node voltages, Q17 looks to be operating on the edge between saturation and active mode, and would likely change into saturation with a large signal amplitude. This is one of the issues with scaling the supply voltage. We will ignore this issue for now (in a real design, you would not be able to do this).

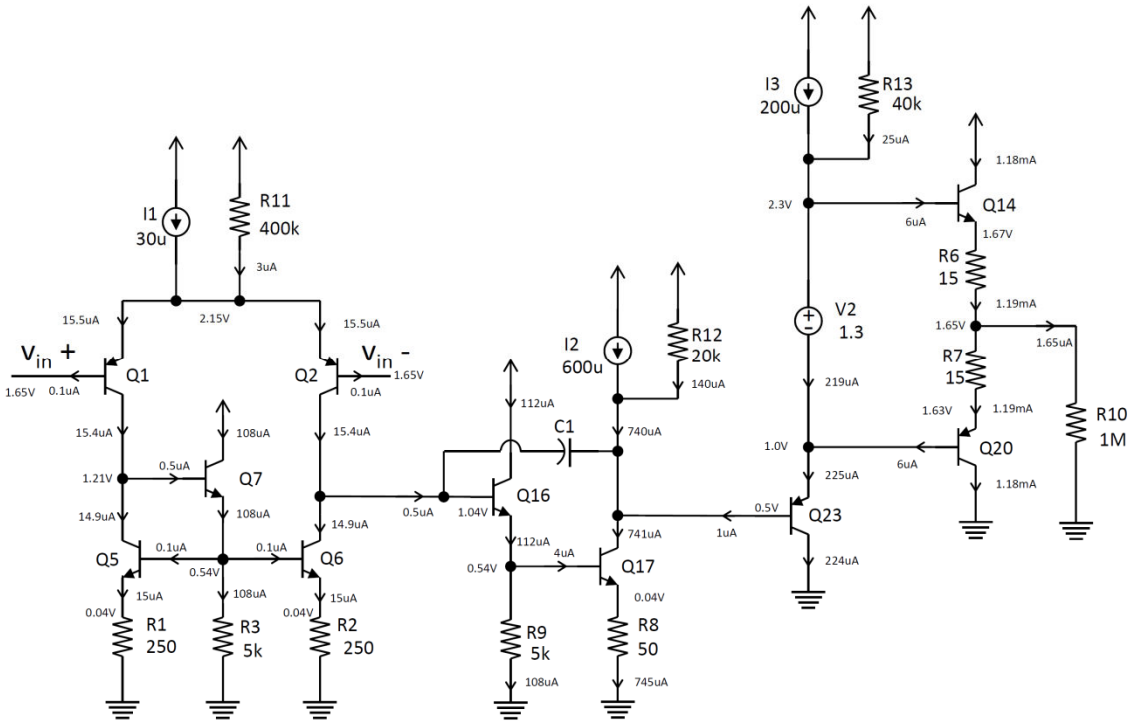


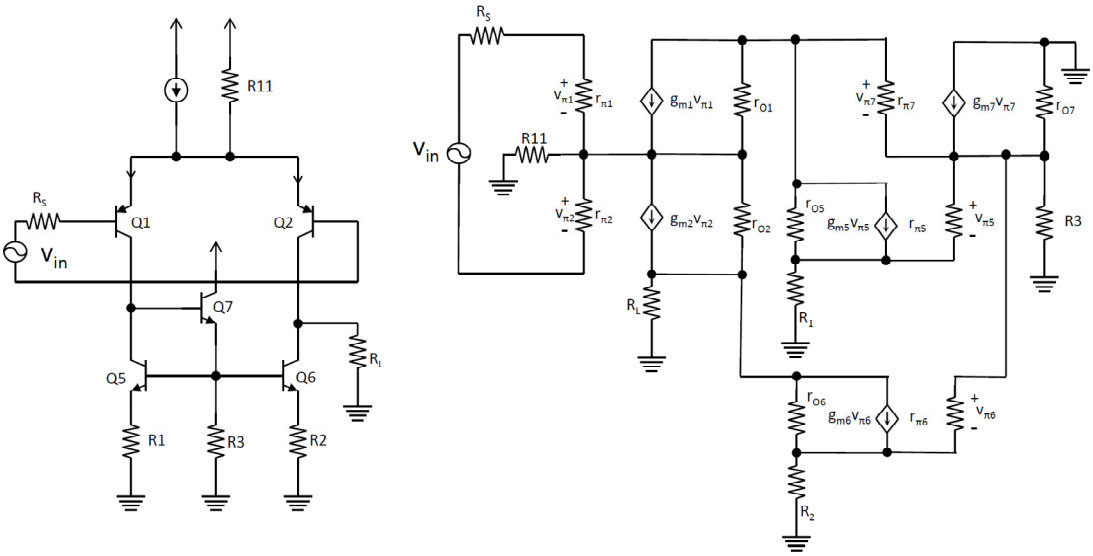
Figure 3.7 Schematic of all stages showing node voltages and line currents

Then, we can fill out the table of DC parameters:

Transistor	I_C (uA)	R_O (Ohm)	g_m (mA/V)
Q1 (PNP)	15.4	649k	0.616
Q2 (PNP)	15.4	649k	0.616
Q5 (NPN)	14.9	2.01M	0.596
Q6 (NPN)	14.9	2.01M	0.596
Q7 (NPN)	108	92.6k	4.32
Q14 (NPN)	1180	25.4k	47.2
Q16 (NPN)	112	89.3k	4.48
Q17 (NPN)	741	40.5k	29.6
Q20 (PNP)	1180	8.47k	47.2
Q23 (PNP)	224	44.6k	8.96

Next, we can perform the small-signal calculations.

We can analyze the circuit as 3 different stages. The only thing we have to keep in mind is that in each analysis, we must model the effects of the other stages. This is done by using linear models: recall that according the linear network theory, we can model any circuit as a single voltage/current source and an impedance (a resistance here since we are dealing with mid-frequency analysis).



First stage

Equivalent circuit of first stage

Figure 3.8 Schematic and small signal equivalent of differential stage

A small signal equivalent of the first circuit can be drawn as seen in Figure 3.8, but is quite complex. This is technically not a problem, as we can solve it even by hand, using some advanced network analysis techniques. The bigger problem is that this complex circuit does not lead to insight. This is an important drawback: in real life, we can always analyze a circuit as precisely as we want by using a simulator (provided we have accurate models and simulation algorithms- a topic for more advanced courses), but knowing what to simulate and what to components change depends on our own understanding of the circuit.

Thus, we need to simplify the circuit substantially in order to figure out the basics for this circuit. This gives us a highly approximate solution, but lets us understand how the characteristics of the circuit are controlled. If we were to then improve the design, we could easily figure out what to do. An exact solution, even if it were tractable, would probably not let us do that.

Let us consider a simple differential pair driving a current mirror with no degeneration resistors and a single-ended load. The circuit and small signal equivalent model is shown in Figure 3.9.

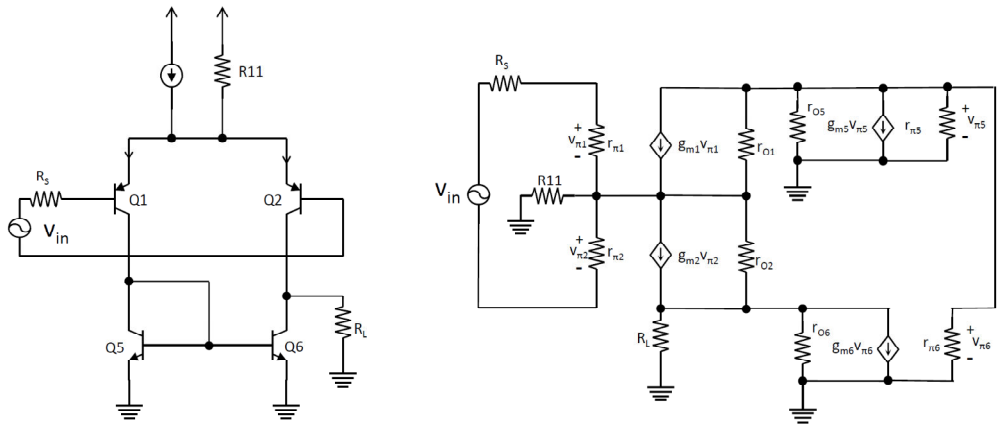


Figure 3.9 Schematic and small signal equivalent of a simple differential pair driving a current mirror and resistive, single ended load

We can make some simplifications: recall that with a differential input, we get a virtual ground. Along this line in the middle, the potential will remain constant without the need for current to flow. Thus, we can remove this line with no impact on the circuit's behavior. This of course means we can remove R_{11} with no impact (no AC current is flowing through it). Also note that R_L and r_{O6} are in parallel. As for Q_5, we can make some more simplifications since the base and collector are shorted:

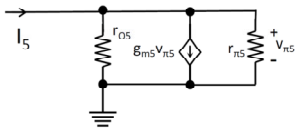


Figure 3.10 Small signal model of Q5 of simple differential pair

$$I_5 = \frac{v_{\pi 5}}{r_{O5}} + \frac{v_{\pi 5}}{r_{\pi 5}} + g_{m5}v_{\pi 5} = \left(\frac{1}{r_{O5}} + \frac{1}{r_{\pi 5}} + g_{m5}\right)v_{\pi 5} = \frac{v_{\pi 5}}{r_{O5}||r_{\pi 5}||\frac{1}{g_{m5}}}$$

And of course, these are parallel with $r_{\pi 6}$.

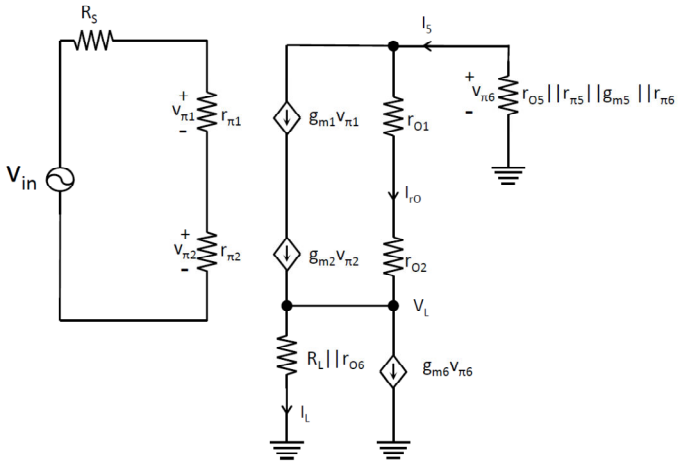


Figure 3.11 Simplified small signal model of the differential pair

We can combine the two trans-conductance modules since both $r_{\pi 1}$ and $r_{\pi 2}$ and g_{m1} and g_{m2} should be identical (a reasonable assumption for a good differential pair) we can combine both. To handle r_{O1} and r_{O2}, we recall that the node connecting the two transistors is a virtual ground, and thus rO1 is in parallel with rO5, rpi5, etc. and rO2 is in parallel with the output impedance of Q6 and the load resistance. We can then calculate the output voltage across the load resistor.

$$V_L = (R_L||r_{O6}||r_{O2})(g_{m2}v_{\pi 2} + -g_{m6}v_{\pi 6})$$

We can eliminate $v_{\pi 6}$ using the following equation:

$$v_{\pi 6} = -(g_{m2}v_{\pi 2})\left(r_{O5}||r_{\pi 5}||\frac{1}{g_{m5}}\right)$$

$$V_L = (R_L||r_{O6}||r_{O2})\left(g_{m2}v_{\pi 2} + g_{m6}(g_{m2}v_{\pi 2})\left(r_{O5}||r_{\pi 5}||\frac{1}{g_{m5}}\right)\right)$$

Next, we note that $\frac{1}{g_{m5}} = r_{e5}$ is much smaller than the resistances it is in parallel with. Also note that $g_{m5} = g_{m6}$ since both transistors should be biased identically:

$$V_L = (R_L||r_{O6}||r_{O2})\left(g_{m2}v_{\pi 2} + g_{m6}(g_{m2}v_{\pi 2})\left(\frac{1}{g_{m5}}\right)\right)$$

$$V_L = 2g_{m2}v_{\pi 2}(R_L||r_{O6}||r_{O2})$$

Now we can look at the input stage and see that

$$v_{\pi 2} = \frac{r_{\pi 2}v_{in}}{R_s + r_{\pi 1} + r_{\pi 2}} = \frac{v_{in}}{2}$$

if we assume the source impedance is very small compared to the op-amp input impedance. This gives us

$$V_L = 2g_{m2}\frac{v_{in}}{2}(R_L||r_{O6}||r_{O2})$$

$$A_{v1} = \frac{V_L}{v_{in}} = g_{m2}(R_L||r_{O6}||r_{O2})$$

If the input impedance of the next stage is very large, are gain is partially limited by r_{O6}. Next, let us see what happens to the effective output impedance of the current mirror branch when we add a degeneration resistor (Note that the base is at virtual ground):

$$I_{out} = \frac{V_{out} + v_{\pi 6}}{r_{O6}} + g_{m6} v_{\pi 6}$$

Also note that we have

$$v_{\pi 6} = -I_{out}(R_2 || r_{\pi 6})$$

which can be used to give

$$I_{out} = \frac{V_{out}}{r_{O6}} - \frac{I_{out}(R_2 || r_{\pi 6})}{r_{O6}} - g_{m6} I_{out}(R_2 || r_{\pi 6})$$

$$I_{out}\left(\frac{r_{O6} + (R_2 || r_{\pi 6}) + g_{m6} r_{O6}(R_2 || r_{\pi 6})}{r_{O6}}\right) = \frac{V_{out}}{r_{O6}}$$

$$R_{out} = \frac{V_{out}}{I_{out}} = r_{O6}\big(1 + g_{m6}(R_2 || r_{\pi 6})\big) + (R_2 || r_{\pi 6})$$

With the given bias point in the first stage of the op-amp, we can get the following:

$$R_{out} = 2.01\text{M}\left(1 + 0.000596\left(250 || \frac{200}{0.000596}\right)\right) + \left(1000 || \frac{200}{0.000596}\right)$$

$$R_{out} = 2.01\text{M}\big(1 + 0.000596(250 || 335570)\big) + (250 || 335570)$$

$$R_{out} = 2.01\text{M}\big(1 + 0.000596(250)\big) + 250 \approx 2.01\text{M}(1.15) = 2.31\text{M}$$

Note that the degeneration resistance improved the output resistance by 15%. For this circuit, the 2M output impedance is already quite large, so there is not much gained by doing this. However, with modern op-amps, the output impedance of a transistor can be 1k or lower, making this technique much more useful. Unfortunately, the degeneration resistor requires a significant voltage drop, which is note easily spared in today's world of low voltage digital optimized IC processes.

As we mentioned earlier, the circuit we have analyzed is not the same as the first stage of our op-amp, but it is close. The main difference is the higher output impedance of the current mirror, as discussed before- just replace the value of r_{06} with the new calculated one. The other difference is the transistor Q_7, but the addition of this transistor causes the first stage current mirror to behave like the simple current mirror we described earlier, although it is still necessary.

Now that we have converted the circuit from differential to single ended, the analysis of the remaining stages is much easier. Below is the circuit and the small signal equivalent model of the second stage. To perform the analysis, we used the T-model for the CC amplifier, which makes things much easier.

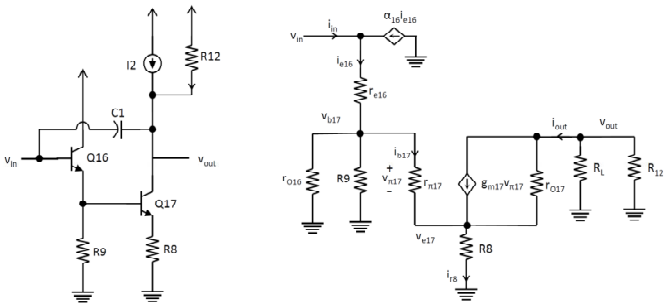


Figure 3.12 Schematic and small signal model of the second stage

We start by first analyzing the CE stage. For the CE stage with degeneration (ignoring r_{O17}):

$$v_{out} = I_{out}(R_L||R_{12})$$

$$I_{out} = g_{m17}v_{\pi 17} = g_{m17}(v_{b17} - v_{e17})$$

$$\frac{v_{e17}}{R_8} = g_{m17}(v_{b17} - v_{e17}) + \frac{v_{b17} - v_{e17}}{r_{\pi 17}}$$

$$\frac{v_{e17}}{R_8} + g_{m17}v_{e17} + \frac{v_{e17}}{r_{\pi 17}} = g_{m17}v_{b17} + \frac{v_{b17}}{r_{\pi 17}}$$

$$\frac{v_{e17}}{R_8||\frac{1}{g_{m17}}||r_{\pi 17}} = \frac{v_{b17}}{\left(r_{\pi 17}||\frac{1}{g_{m17}}\right)}$$

$$v_{e17} = v_{b17}\frac{R_8||\frac{1}{g_{m17}}||r_{\pi 17}}{\left(r_{\pi 17}||\frac{1}{g_{m17}}\right)}$$

$$I_{out} = v_{b17}g_{m17}\left(1 - \frac{R_8||\frac{1}{g_{m17}}||r_{\pi 17}}{r_{\pi 17}||\frac{1}{g_{m17}}}\right)$$

$$I_{out} = v_{b17}\frac{g_{m17}}{1 + R_8 g_{m17} + \frac{R_8}{r_{\pi 17}}}$$

$$v_{out} = v_{b17}\frac{g_{m17}(R_L||R_{12})}{1 + R_8 g_{m17} + \frac{R_8}{r_{\pi 17}}}$$

Next for the input impedance of the CE stage:

$$i_{b17} = \frac{v_{b17} - v_{e17}}{r_{\pi 17}} = v_{b17}\frac{1 - \frac{R_8||\frac{1}{g_{m17}}||r_{\pi 17}}{r_{\pi 17}||\frac{1}{g_{m17}}}}{r_{\pi 17}}$$

$$i_{b17} = v_{b17}\frac{1}{r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17}}$$

$$R_{in} = \frac{v_{b17}}{i_{b17}} = r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17}$$

Next we can calculate the effect of the CC stage, which lets us calculate the gain:

$$\frac{v_{b17}}{v_{in}} = \frac{r_{O16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17})}{r_{e16} + r_{O16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17})}$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_{b17}}\frac{v_{b17}}{v_{in}} = \frac{r_{O16}||R_9||(r_{\pi17} + R_8 + r_{\pi17}R_8g_{m17})}{r_{e16} + r_{O16}||R_9||(r_{\pi17} + R_8 + r_{\pi17}R_8g_{m17})}\frac{g_{m17}(R_L||R_{12})}{1 + R_8g_{m17} + \frac{R_8}{r_{\pi17}}}$$

We also need the input impedance:

$$i_{in} = i_{e16} - \alpha i_{e16} = i_{e16}(1-\alpha) = i_{e16}\left(1 - \frac{\beta}{\beta+1}\right) = \frac{i_{e16}}{\beta+1}$$
$$v_{in} = i_{e16}\left(r_{e16} + r_{O16}||R_9||(r_{\pi17} + R_8 + r_{\pi17}R_8g_{m17})\right)$$
$$R_{in} = \frac{v_{in}}{i_{in}} = (\beta+1)\left(r_{e16} + r_{O16}||R_9||(r_{\pi17} + R_8 + r_{\pi17}R_8g_{m17})\right)$$

Finally, we can consider the last stage. Again, we draw the small signal equivalent model. Note that again we use the T-model, and that we have omitted rO for all transistors for simplicity. We will need to put them back when we find the output impedance.

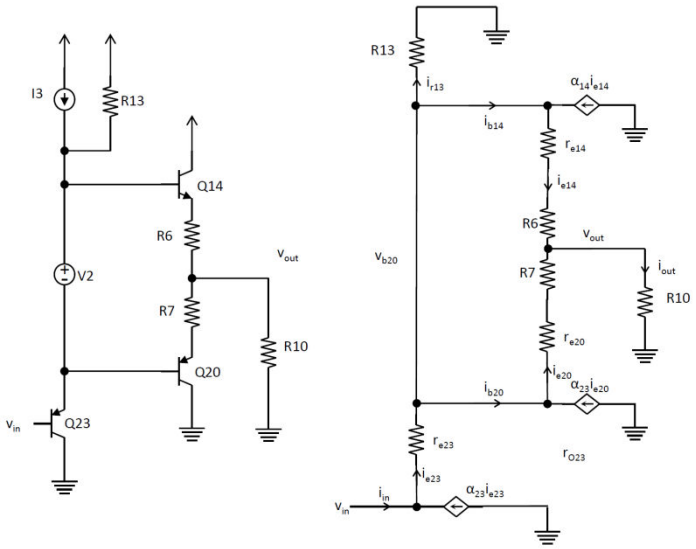


Figure 3.13 Schematic and small signal model of the third stage

First, we find the input impedance of the second set of CC amplifiers:

$$v_{out} = i_{out}R_{10}$$
$$i_{out} = i_{e14} + i_{e20} = (\beta+1)i_{b14} + (\beta+1)i_{b20}$$
$$v_{b20} - v_{out} = i_{e14}(r_{e14} + R_6) = i_{e20}(r_{e20} + R_7)$$
$$(\beta+1)i_{b14} = (\beta+1)i_{b20}\frac{r_{e20} + R_7}{r_{e14} + R_6}$$
$$i_{b14} = i_{b20}\frac{r_{e20} + R_7}{r_{e14} + R_6}$$
$$R_{in} = \frac{v_{b20}}{i_{b14} + i_{b20}} = \frac{v_{out} + v_{b20} - v_{out}}{i_{b14} + i_{b20}} = \frac{i_{out}R_{10} + i_{e20}(r_{e20} + R_7)}{i_{b20}\frac{r_{e20} + R_7}{r_{e14} + R_6} + i_{b20}}$$
$$R_{in} = \frac{\left((\beta+1)i_{b14} + (\beta+1)i_{b20}\right)R_{10} + (\beta+1)i_{b20}(r_{e20} + R_7)}{i_{b20}\frac{r_{e20} + R_7}{r_{e14} + R_6} + i_{b20}}$$
$$R_{in} = (\beta+1)\frac{\left(\frac{r_{e20} + R_7}{r_{e14} + R_6} + 1\right)R_{10} + (r_{e20} + R_7)}{\frac{r_{e20} + R_7}{r_{e14} + R_6} + 1}$$

$$R_{in} = (\beta + 1)\frac{R_{10}(r_{e20} + R_7 + r_{e14} + R_6) + (r_{e14} + R_6)(r_{e20} + R_7)}{r_{e20} + R_7 + r_{e14} + R_6}$$

$$R_{in} = (\beta + 1)\left(R_{10} + \frac{(r_{e14} + R_6)(r_{e20} + R_7)}{r_{e20} + R_7 + r_{e14} + R_6}\right)$$

$$R_{in} = (\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)$$

From v_{b20}, the impedance to ground is just this impedance in parallel with R_{13}.

$$R = (\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}$$

Note that because the beta values are the same for both PNP and NPN transistors, we can consider to two output paths to be parallel. As such, we can easily find the voltage gain from v_{b23} to the output:

$$\frac{v_{out}}{v_{b20}} = \frac{R_{10}}{R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)}$$

The gain for the first stage is just a normal CC, so we can determine the gain and input impedance easily:

$$\frac{v_{b20}}{v_{in}} = \frac{(\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}}{r_{e23} + (\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}}$$

$$A_{v3} = \frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_{b20}}\frac{v_{b20}}{v_{in}}$$

$$A_{v3} = \frac{R_{10}}{R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)}\frac{(\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}}{r_{e23} + (\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}}$$

Of course, this gain will always be less than 1.

$$R_{in3} = (\beta + 1)\big(r_{e23} + (\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}\big)$$

$$R_{in3} = (\beta + 1)r_{e23} + (\beta + 1)\Big((\beta + 1)\big(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)\big)||R_{13}\Big)$$

It can be seen that, if R_{13} is large enough, the double amplifier stage increases the output impedance by a factor of β^2.

As described in your notes, the capacitor C_1 is added deliberately to provide a dominant pole, which in turn determines the frequency response of the entire circuit. Just as with a transistor, the frequency at which the gain becomes 1 can be calculated:

$$\omega_T = A_0\omega_p$$

Where A_0 is the low frequency gain and ω_p is the pole frequency.

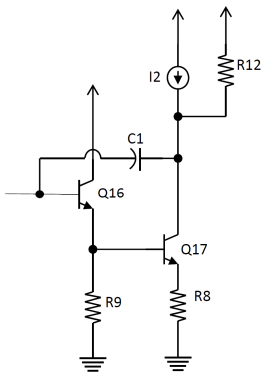


Figure 3.14 Schematic showing the position of C_1 in the second stage of the op-amp

As can be seen in the circuit above, C1 links the output and input of the second stage. Assuming a large second stage gain, we can use the Miller multiplication to convert C1 into 2 equivalent capacitances. Due to the large gain of the second stage, the dominant pole is formed by the first capacitance.

$$C_A = C_1\left(1 - \frac{v_{c17}}{v_{b16}}\right) = C_1(1 + A_{v2})$$

This capacitance is in parallel with the input impedance of the second stage and the output impedance of the first stage. The first value was calculated already, and the second value can be determined by the output impedance of the degenerated current mirror created by Q16. Then, our pole frequency can be calculated

$$\omega_p = \frac{1}{C_A(R_{out1}||R_{in2})}$$

The slew rate can be determined by measuring the fastest rate of change of the amplifier. To perform this kind of test, we connect the op-amp in as a unity gain buffer:

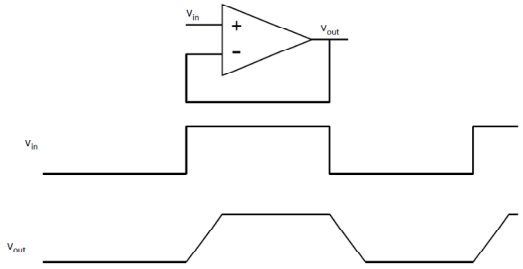


Figure 3.15 Schematic of the op-amp connected as a buffer and 2 sample input and output waveforms

For this analysis, the input signal is large in magnitude, and so we cannot use the simple linear models, but must instead consider the large signal models (the same ones we use for DC calculations).

The schematic below shows parts of the op-amp. With a large input spike, the BE junction of the first transistors is immediately decreased sharply, causing the transistor to enter into the cutoff mode, effectively shutting it off. The current flowing through the current source attempts to remain constant, so all the current must flow through Q_2. Note that as the left branch no

longer has any current flowing through it, Q_6 will shut off and by extension, Q7 since they share the same base voltages. Thus, all the current must flow into the input of the second stage.

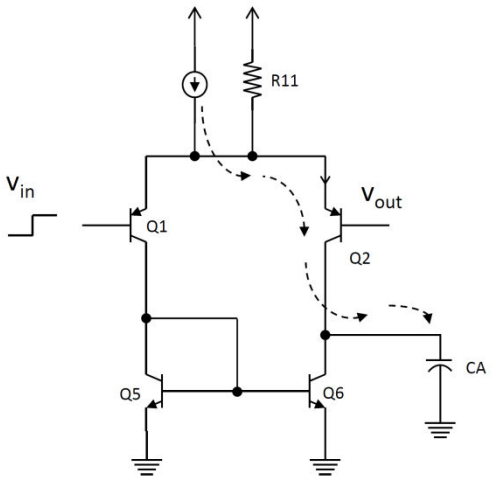


Figure 3.16 Schematic of op-amp circuit showing used for analysis of slew rate

The reaction speed of the circuit is limited by the presence of C1. When we use the Miller model, it is obvious that the fastest rate of change occurs when all of the current flows into C_A: because of the huge size of C_A, this is a good assumption. This gives us the rate of change for the input of the second node, but not the output. But we know that the output of the second stage compared to the input is simply A_{V2}, and the gain of the third stage is approximately 1. Note that the gain of the second stage increases the effective capacitance, so it is cancelled out. Thus:

$$\frac{\Delta V_{out1}}{\Delta t} = \frac{I_1}{C_A}$$

$$\frac{\Delta V_{out2}}{\Delta t} = A_{V2}\frac{\Delta V_{out1}}{\Delta t} = A_{V2}\frac{I_1}{C_A} = A_{V2}\frac{I_1}{A_{V2}C_1} = \frac{I_1}{C_1}$$

$$\text{slew rate} = \frac{\Delta V_{out3}}{\Delta t} = \frac{\Delta V_{out2}}{\Delta t} = \frac{I_1}{C_1}$$