The goal of this project is to design a chip that could control a bicycle taillight to produce an apparently random flash sequence. The chip should operate from a 3 V supply (two AA batteries in series).

The heart of the chip will be a 5-bit pseudorandom sequence generator (PRSG). This device produces a bit stream that appears random, but repeats after $2^5 - 1 = 31$ bits. A basic block diagram for the PRSG is shown in Fig. 1. PHI is an input clock.

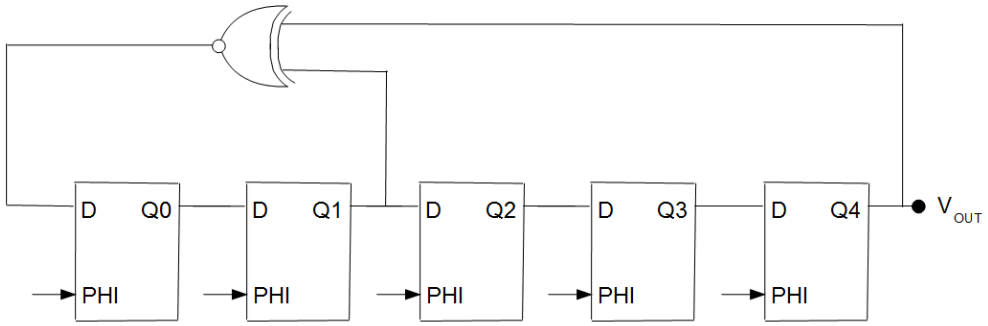


Fig. 1 Pseudorandom sequence generator implemented with shift register and feedback.

The PRSG contains five D flip-flops cascaded to make a shift register. In the baseline project the D flip-flops are made with dynamic logic. In this alternative project the D flip-flops will be made using textbook classic static logic gates as shown in Fig. 2 below. This requires far more transistors for an individual flip-flop (36 versus 4!) but saves space by not needing a 2-phase clock generator (14 transistors) or, more importantly, room for two clock distribution lines rather than just one. The static D flip-flop is also not sensitive to off-state leakage problems in the MOSFETs.

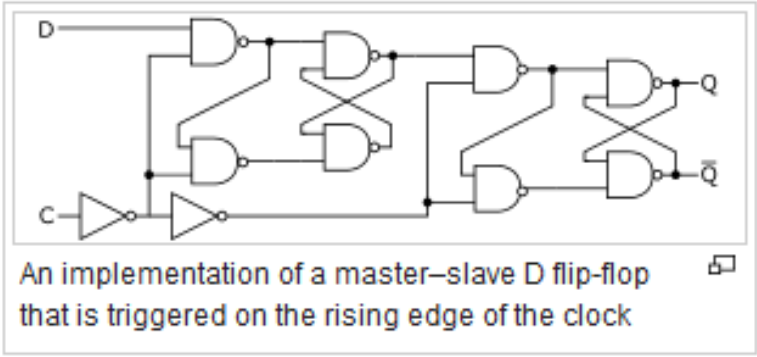


Fig. 2 Shift register stage implemented using static CMOS gates (stolen from Wikipedia).

The PRSG requires an XNOR logic block. The textbook static logic gate XNOR shown in Fig. 3(a) below is recommended. The circuit of Fig. 3(b) includes a reset function. This is needed since the PRSG of Fig. 2 can enter a "locked" state if every register holds a logic 1. When RESET is high the NOR gate in Fig. 3(b) forces a "0" into the register.

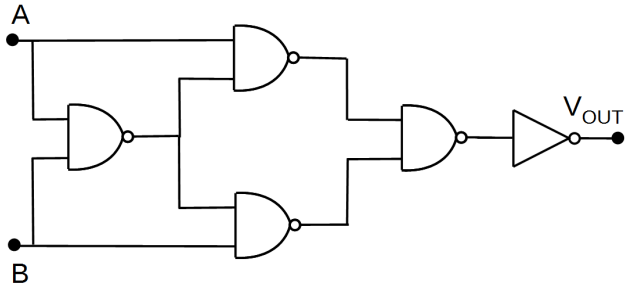
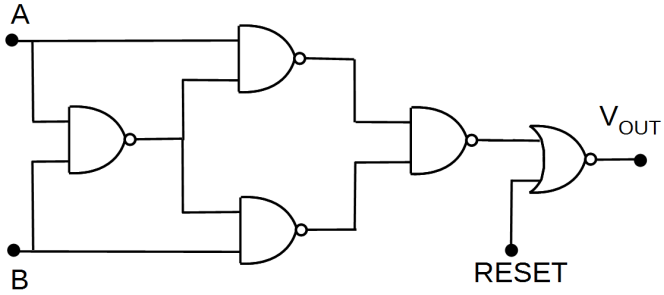


Fig. 3 (a) XNOR using static logic gates



(b) XNOR with reset capability

. An on-chip master clock generator is desirable. A suitable oscillator circuit that can be used to generate the clock is shown in Fig. 4.

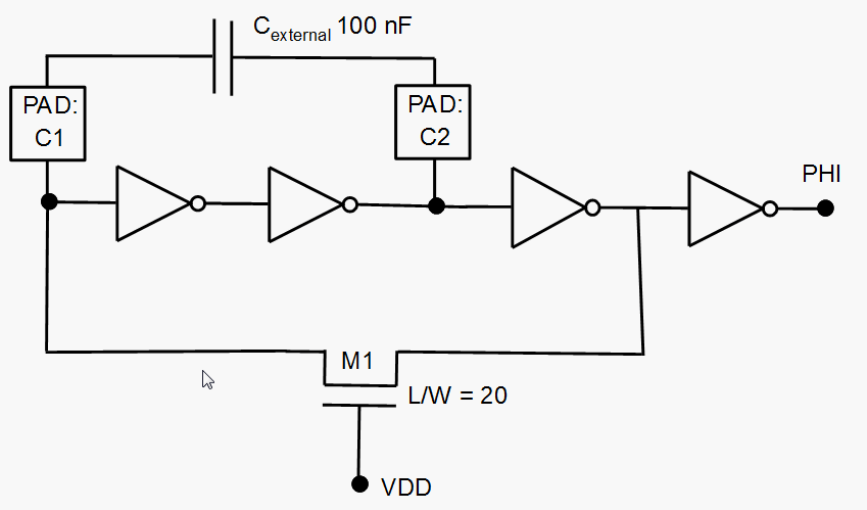


Fig. 4 Master clock generator- external capacitor $C_{external}$ and resistance of M1 determine frequency

$C_{external}$ is an external capacitor connected across two bond pads in the circuit. Values of $C_{external}$ between about 10 and 500 nF will be used for testing (capacitance values larger than about 10 pF are difficult to realize on-chip). For initial testing using an oscilloscope to observe the output waveform a relatively small $C_{external}$ giving a clock frequency of a few kHz is appropriate. For use in a bike taillight, the clock needs to be sufficiently slow that the LED flash rate is approximately 10 Hz, so that a human eye can see the flash. $C_{external}$ can be adjusted to give the flash rate you think will be most visible. For initial simulations, try $C_{external}$ = 1 nF.

If the clock generator fails, or if we wish to test at higher clock frequencies than can be provided by the oscillator of Fig. 4 an external clock can be injected at bond pad C2.

The complete chip should include an output buffer able to drive a GaP red LED. A typical red LED has a turn-on voltage of about 2 V and draws about 10 mA. A possible SPICE model for such an LED is given below.

```
.model Di_LED D (IS=4e-20 RS=0 BV=5 IBV=100u CJO=0 M=0.5 N=2)
```

The output buffer might consist of a single wide nMOS transistor in “open drain” configuration, as shown in Fig. 5. The driver transistor M1 must be able to sink 10 mA with V_{DS} = 1 V and V_{GS} -= 3V.

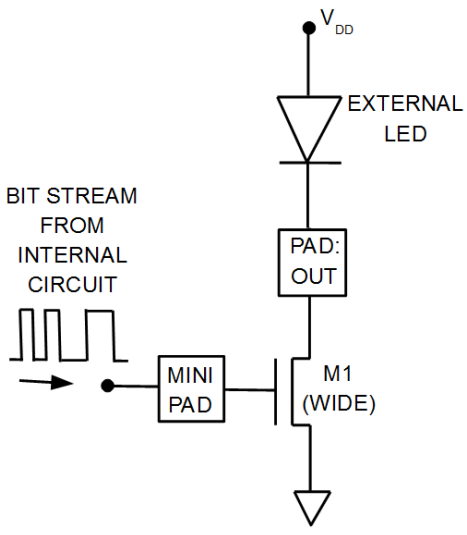


Fig. 5 Open drain output buffer

The complete project should fit in the floor plan shown in Fig.6. The height of the project block is fixed at 240 λ, and must not be changed. The vertical position of the bond pad centers must also not be changed. The width of the project should be kept as small as possible.

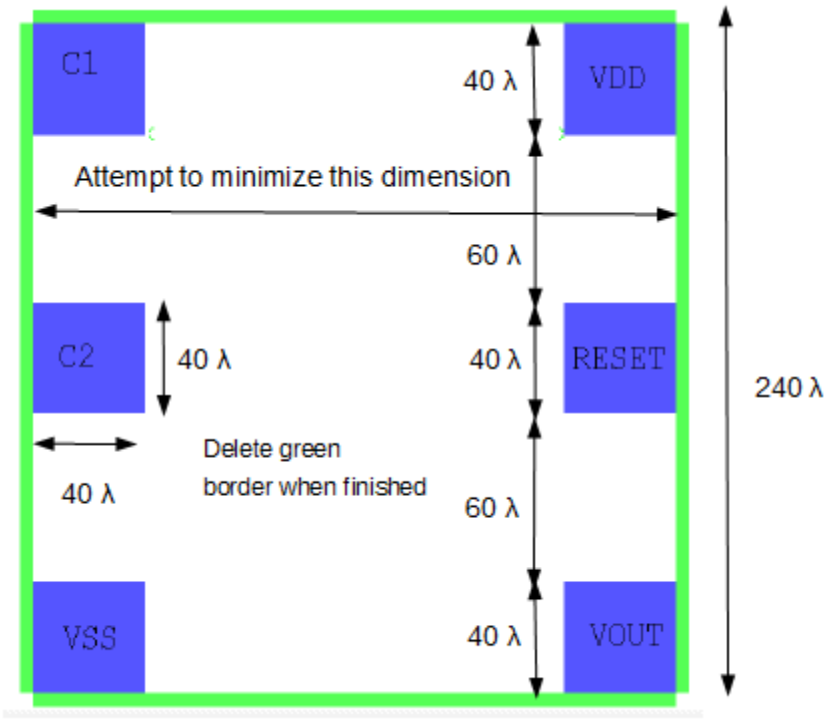


Fig. 6 Probe pad placement and available area for layout

Since the static D flip-flop of Fig. 3 will take far more area than the dynamic flip-flop used in the baseline project, there might not be room for all five stages in the shift register. If this is the case it's acceptable to use four stages.