

**Instructor:** N. Garry Tarr ME5160 email: [ngt@doe.carleton.ca](mailto:ngt@doe.carleton.ca)

**TAs:** Alex Ross ME5135 email: [AlexJRoss@cmail.carleton.ca](mailto:AlexJRoss@cmail.carleton.ca)  
Samantha Trifoli ME5138 email: [samanthatrifoli@cmail.carleton.ca](mailto:samanthatrifoli@cmail.carleton.ca)

**Course web site:** <http://www.doe.carleton.ca/~ngt/4609> username: 4609 password:

**Marking scheme:** Final exam 50% (*The final exam is for evaluation only and will not be returned*)  
IC design project 50% (*Passing grade in project required to obtain credit for course*)

### IC Design Project

A major component of ELEC4609 is the design and testing of a simple CMOS integrated circuit. We will attempt to fabricate the circuits here at Carleton, and return finished silicon chips for testing before the end of term. Students are encouraged to work in pairs on the project, but must submit individual reports. In order to allow time for chip fabrication, there will be a tight deadline for design submission of **February 13**. A complete layout with full supporting simulation results must be submitted at this time to obtain credit for the course. A comprehensive report, due towards the end of term, is expected on this project. Guidelines for report preparation will be provided later.

### Assignments and Labs

The IC design project requires many, many hours of work with CAD tools, and inevitably much of this work will be done outside scheduled lab periods. It's possible to work at home or in any of the DOE undergrad computer labs. The formally scheduled lab periods provide an opportunity to have the TA review and comment on your work. The first two lab sessions will provide a tutorial introduction to the CAD tools we will use. In addition to the term IC design project, there will be an assignment (not marked, but covered on the final exam) on the fundamentals of CMOS process design. Labs begin Jan. 8.

### Topics:

#### 1. Basic MOS IC Design Concepts

Basic CMOS structure and process flow. Relationship between layout and cross-section. Design rules.

#### 2. MOS Circuit Building Blocks

CMOS inverter: transfer characteristic, ratioing, noise margin, rise and fall times. Advantages of CMOS. NAND and NOR gates. Transmission gates. Dynamic logic. Input protection. Driving large capacitive loads with output buffers. Latch-up. Introduction to analog CMOS circuits: differential amplifiers, source follower buffers, current mirrors, device matching, temperature compensation.

#### 3. MOS Process Technology Steps

Overview of the processes required to fabricate a MOS IC: oxidation, ion implantation, diffusion, thin film deposition, photolithography and etching. Integration of basic steps into a simple CMOS process flow.

#### 4. Advanced CMOS Technology (as time permits)

Short channel effects, hot carrier effects and techniques for suppression. Evolution of CMOS technology: shallow trench isolation, high-k dielectrics, strained silicon... The future of microelectronics.

### Recommended (but not compulsory) textbook:

R. Jacob Baker, Harry W. Li, and David E. Boyce, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed, 2010 IEEE Press, ISBN 0-7803-3416-7 (can be ordered online through IEEE or Chapters)

**Health and Safety:** See <http://www.doe.carleton.ca/undergrads/health-and-safety.pdf> for general guidelines. Normal precautions in working with low-voltage electrical equipment must be taken when testing projects. Students volunteering to assist in multiproject chip fabrication in the Carleton Microfab must complete special training, and must be WHMIS qualified.