Name: ________________________________ Student Number: _________

CARLETON UNIVERSITY

FINAL EXAMINATION April 2015

DURATION: 3 **HOURS** **Number of Students: 21**

Department Name & Course Number: ELEC 4609 Section A

Course Instructors: N.G. Tarr

Authorized Memoranda: Non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has nine (9) pages.

This examination question paper **may not** be taken from the examination room.

In addition to this question paper, students require: an examination booklet yes ☐ no ☐
a Scantron sheet yes ☐ no ☐

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

SEE LAST TWO PAGES OF EXAM FOR DATA AND FORMULAS

WRITE YOUR NAME AND STUDENT NUMBER ON EACH PAGE

Question	Mark
1	
2	
3	
4	
5	
6	
Total	

Name: ________________________________ Student Number: _________

1. Fig. 1.1 on p. 7 shows the layout of a circuit fabricated in an n-well CMOS technology similar to that used in Lab 2. The layout is not complete: the p+ mask is not shown. Draw the outline of this region (or regions) on the layout, and indicate the interior of the region. (*Note*: In this CMOS technology, by default any region that is not covered by the p+ layer receives the n+ implant) *4 marks*

2. In the space provided next to the layout in Fig. 1.1, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *16 marks*

3. a) Underneath the layout of Fig. 1.1, draw the circuit schematic corresponding to the layout. Show the substrate (body) connection for each transistor. *12 marks*

   b) Determine the W/L ratio for each transistor and write it on the circuit schematic. *2 marks*

   c) On the circuit schematic, circle the transistors that are subject to the body effect. *2 marks*

   d) Complete the timing diagram in Fig. 1.2 on p. 7. Briefly explain your answer. *10 marks*

4. Silicon-on-Insulator (SOI) CMOS is immune to latch-up. Explain why *5 marks*

Name: ______________________________ Student Number: _________

5. Fig. 5.1 shows the schematic for a simple circuit built in the bulk CMOS technology of Lab 2. In the following assume $V_{Tn} = -V_{Tp} = 0.5$ V and $\mu_n = 2\mu_p$. All transistors have length $L = 2$ µm. The gate oxide thickness $t_{ox} = 25$ nm. $V_{DD} = 3$ V. The interconnect line between the two inverters in Fig. 5.1 is very short, so that it has negligible capacitance. There is no load of any kind on the second inverter. Assume source and drain junction capacitances are negligible.

a) If the nMOS transistors have width $W_n = 8$ µm, what width W_p is required for the pMOS transistors to give symmetric rise and fall times at node A? Explain briefly. Use this value for W_p in the remaining parts of the question. *5 marks*

b) Suppose V_{in} has been low (0 V) for a long time, then almost instantaneously switches high (V_{DD}). How fast does V_A fall (in other words, what is dV_A/dt) immediately after V_{in} rises? *10 marks*

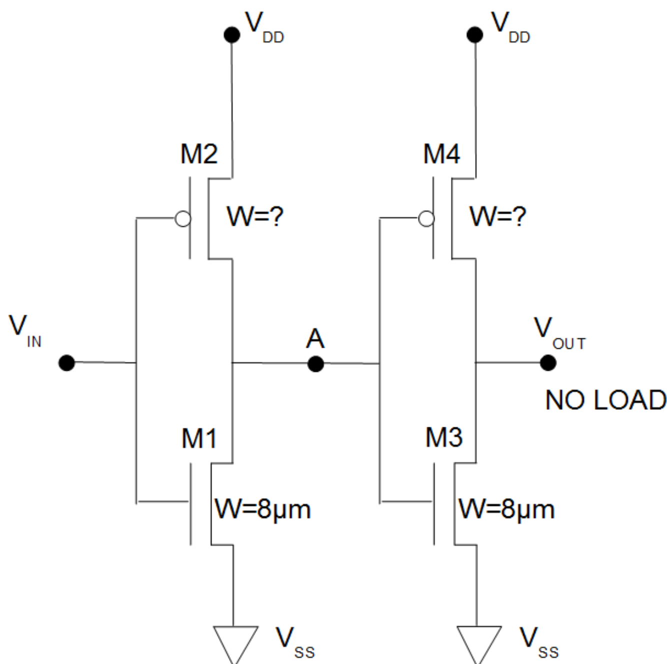


Fig. 5.1

Name: ______________________________ Student Number: _________

c) Approximately how much energy (in Joules) is dissipated in the circuit when V_{in} switches through a complete cycle, from low to high and then back to low? *4 marks*

d) Suppose the circuit of Fig. 5.1 is shrunk by reducing L while keeping all W/L ratios constant. Assume V_{Tn}, V_{Tp}, V_{DD} and t_{ox} are unchanged. We expect the maximum frequency at which the circuit can be clocked to be proportional to $1/L^2$. Explain why. (*Hint:* generalize the solutionto part (b) of this question) *5 marks*

Name: ________________________________ Student Number: _________

6. A simple bulk CMOS technology uses lightly-doped 5 Ωcm n-type starting wafers. A p-well is formed by low-energy boron implantation followed by diffusion to give a surface concentration $N_{A,surf} = 10^{16}$ cm^{-3} and a metallurgical junction depth of 4 µm. Both nMOS and pMOS transistors use polysilicon gates doped to solid solubility with phosphorus. There is NO active device threshold adjust implant.

a) What gate oxide thickness is required to give $V_{Tn} = 0.5$ V?. *10 marks*

b) What boron implant dose is required to form the p-well? *10 marks*

Name: _______________________________ Student Number: _________

c) The factory would like the p-well diffusion to last 16 hours, so that it can run overnight. What temperature (in °C) is required for the diffusion? *3 marks*

d) What is the sheet resistance of the p-well? *2 marks*

Name: ________________________________ Student Number: _________

Cross-Section:

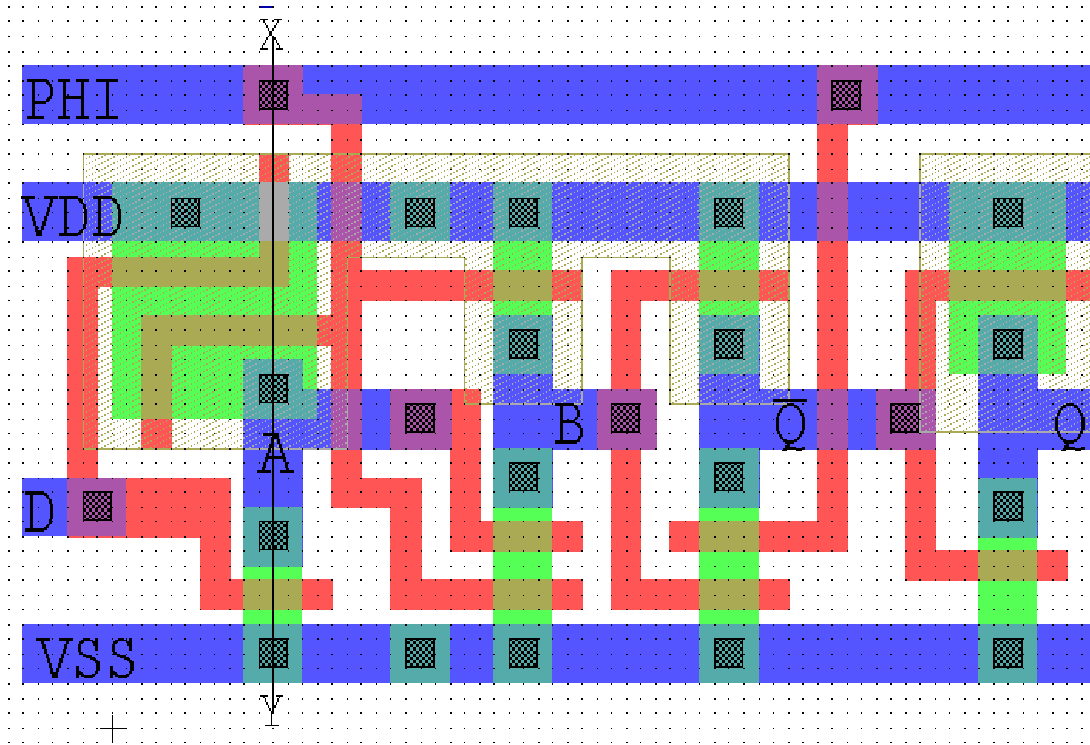


Fig. 1.1

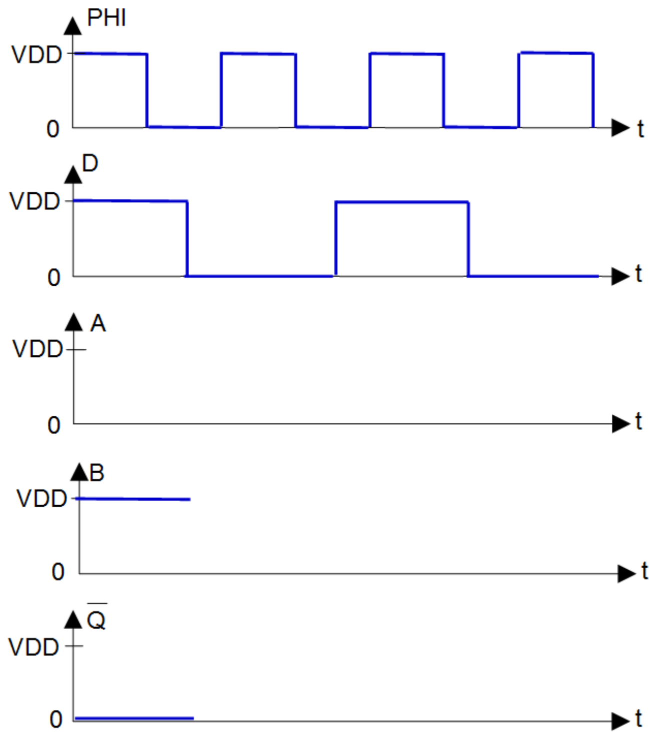


Fig. 1.2 Timing diagram for Fig. 1.1

Name: ________________________________ Student Number: _________

Equations and Constants

Physical constants: q = 1.6x10^{-19} C k = 1.38x10^{-23} JK^{-1} ε_0 = 8.85x10^{-12} Fm^{-1} = 8.85x10^{-14} Fcm^{-1}
1eV = 1.6x10^{-19} J kT/q = 0.0259 V at room temperature 0°C = 273K

Data for silicon at 300K: n_i = 10^{10} cm^{-3} E_G = 1.12 eV N_C = 2.8x10^{19} cm^{-3} N_V = 1x10^{19} cm^{-3}
$\varepsilon_s = 11.9\varepsilon_0$ μ_n = 1350 cm^{2}V^{-1}s^{-1} μ_p = 480 cm^{2}V^{-1}s^{-1} $\varepsilon_{ox} = 3.9\varepsilon_0$
in lightly doped material μ_n = 1350 cm^{2}V^{-1}s^{-1} μ_p = 480 cm^{2}V^{-1}s^{-1}

nMOS threshold voltage: $V_{Tn} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_A}{n_i})$ and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

pMOS threshold voltage: $V_{Tp} = V_{FB} - 2\phi_B - \frac{\sqrt{2\varepsilon_s q N_D (2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_D}{n_i})$

Resistivity: $\rho = \frac{1}{q\mu N}$

Saturation drain current: $I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_T)^2}{2}$

Triode drain current: $I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$

In the following Q_{impl} is the implanted dopant dose (ions/cm^2):

Drive-in diffusion profile: $C(x) = \frac{Q_{impl}}{\sqrt{\pi D t}} e^{-x^2/(4Dt)}$

Ion implant profile: $C(x) = \frac{Q_{impl}}{\sqrt{2\pi}\,\Delta R_P} e^{-(x-R_P)^2/(2\Delta R_P{}^2)}$

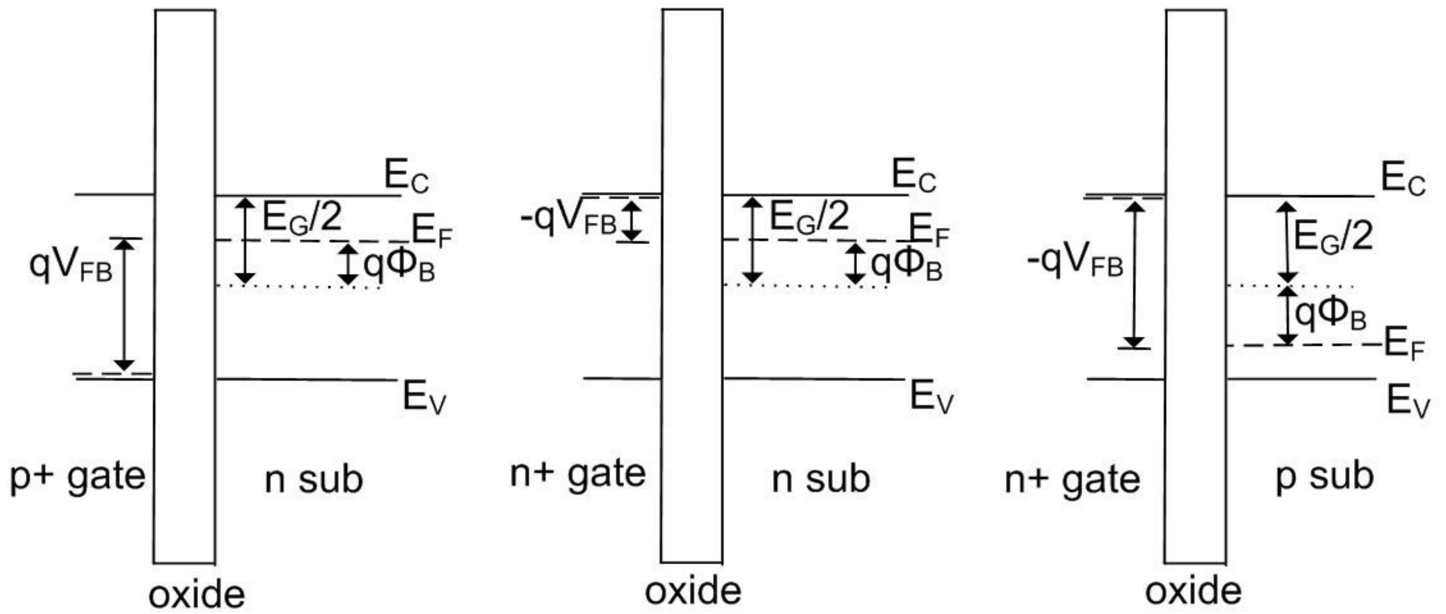
Sheet resistance: $R_S \approx \frac{1}{q\mu Q_{impl}}$

Diffusion coefficient: $D = D_0 e^{-E_A/kT}$ ("Intrinsic" diffusion coefficient for lightly-doped material)

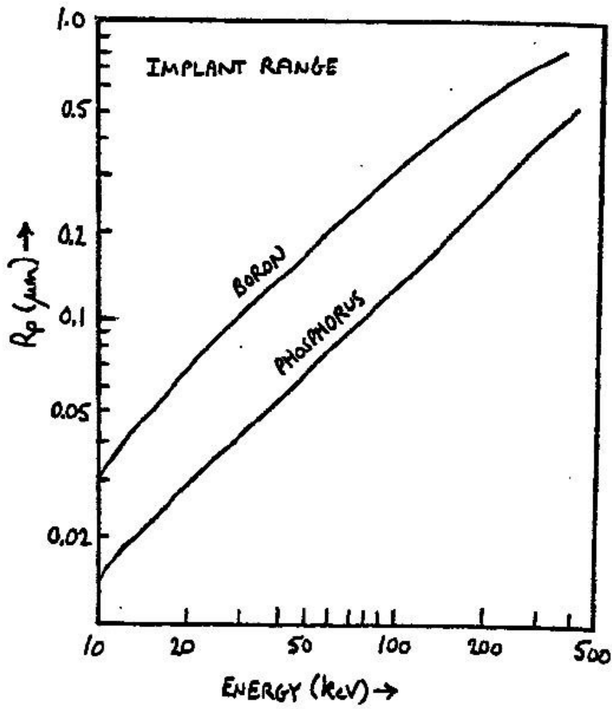
Boron: D_0 = 1.0 cm^{2}s^{-1} E_A = 3.5 eV Phosphorus: D_0 = 4.7 cm^{2}s^{-1} E_A = 3.68 eV

Name: ______________________________ Student Number: _________

Graphical Data



Diagrams for V_{FB} calculation



Implant range and straggle
(assume straggle is equal to range: $\Delta R_P = R_P$)