Name: ______________________________ Student Number: _________

CARLETON UNIVERSITY

FINAL EXAMINATION April 2014

DURATION: 3 **HOURS** **Number of Students:** 38

Department Name & Course Number: ELEC 4609 Section A

Course Instructors: N.G. Tarr

Authorized Memoranda: Non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has ten (10) pages.

This examination question paper **may not** be taken from the examination room.

In addition to this question paper, students require: an examination booklet yes ☐ no ☐
a Scantron sheet yes ☐ no ☐

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

SEE LAST TWO PAGES OF EXAM FOR DATA AND FORMULAS

WRITE YOUR NAME AND STUDENT NUMBER ON EACH PAGE

Question	Mark
1	
2	
3	
4	
5	
6	
Total	

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1. Fig. 1.1 on p. 8 shows the layout of a circuit fabricated in the n-well CMOS technology similar to that used in Lab 2. The layout is not complete: the p+ mask is not shown. Draw the outline of this region (or regions) on the layout, and use cross-hatching to indicate the interior of the region. (*Note*: In this CMOS technology, by default any region that is not covered by the p+ layer receives the n+ implant) *4 marks*

2. In the space provided next to the layout in Fig. 1.1, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *16 marks*

3. a) Underneath the layout of Fig. 1.1, draw the circuit schematic corresponding to the layout. Show the substrate (body) connection for each transistor. *8 marks*

   b) Determine the *W*/*L* ratio for each transistor and write it on the circuit schematic. *2 marks*

   c) On the circuit schematic, circle the transistors that are subject to the body effect. *2 marks*

   d) Complete the timing diagram shown in Fig. 3.1 below. Briefly explain your answer. *7 marks*

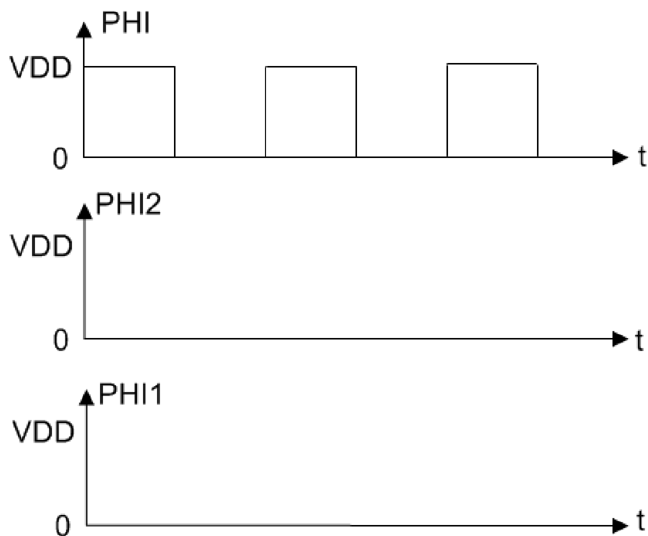

Fig. 3.1 Timing diagram for Fig. 1.1

   e) In the layout of Fig. 1.1, is intermediate output A at midrail ($V_{DD}/2$) when the input PHI is midrail? Explain. *3 marks*

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f) The layout of Fig. 1.1 has been designed to give equal rise and fall times for outputs PHI1 and PHI2 when driven by a square wave input clock PHI. However, this has been accomplished at the expense of a large layout area. Sketch a schematic for an alternative circuit that could provide the same logic function as Fig. 1.1 and also provide symmetric rise and fall times when driven by a square wave input clock, but use a smaller layout area without reducing switching speed. No layout is required, just the schematic. *8 marks*

4. The layout of Fig. 1.1 is prone to latch-up. Describe how the layout should be modified to improve latch-up immunity. Draw a sketch to illustrate your answer if you wish. *5 marks*

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5. Fig. 5.1 shows an incomplete circuit schematic for a simple op-amp stage made in the n-well CMOS technology of Lab 2. Here an inverter formed by M8 and M9 serves as a final gain stage. In the following assume $V_{Tn} = -V_{Tp} = 0.7$ V and $\mu_n = 2\mu_p$

   a) For the bias conditions specified in Fig. 5.1, what is the DC level V_X at node X? Show the steps in your solution. Ignore the body effect. *9 marks*

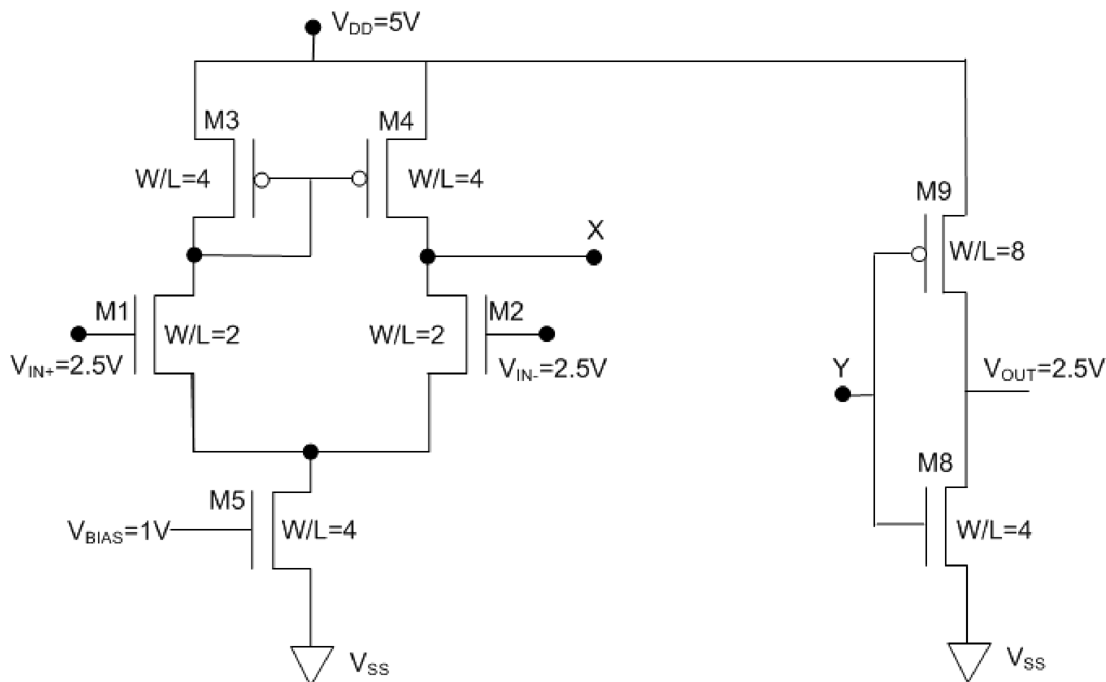

Fig. 5.1

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b) Complete the schematic of Fig. 5.1 by adding a level shifter stage to connect node X and node Y. The level shifter should give $V_{out} = 2.5$ V when $V_{in+} = V_{in-} = 2.5$V. Compute the W/L ratios required for the transistors in the level shifter. The V_{bias} supply shown in Fig. 5.1 may be used in the level shifter. Briefly explain your work. *9 marks*

c) Confirm that transistor M2 in Fig. 5.1 is in saturation. *2 marks*

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6. Very early CMOS technologies often used lightly-doped n-type starting material. The outline for such a process follows (here "PE" refers to a photolithography step):

Starting material: 5 Ωcm n-type (100) orientation

A. P- well formation

1. First mask oxidation t_{ox}=200 nm T=1000°C time=30 min wet O_2
2. p-well P.E. and oxide etch **PE 1**
3. p-well implant boron dose=$2x10^{12}$ cm^{-2} energy=50 keV
4. Well drive-in T=1150°C time=10 hours dilute O_2 in Ar

B. Device Isolation

1. Blanket oxide etchback
2. Pad oxidation t_{ox}=50 nm T=1000°C time=1 hour dry O_2
3. Nitride deposition $t_{nitride}$=80 nm
4. Device well P.E. and nitride etch **PE 2**
5. Field oxidation t_{ox} =1 μm T=1000°C time=5 hours wet O_2

C. Active device formation

1. Blanket nitride and pad oxide etchback
2. Gate oxidation t_{ox}=50 nm T=1000°C time = 1 hour dry O_2
3. Gate polysilicon deposition t_{poly}=0.35 μm
4. Blanket poly doping phosphorus (solid solubility chemical source) T=950°C
5. Polysilicon gate P.E. and etch **PE 3**
6. Gate oxide etchback (remove all oxide)
7. n+ PE **PE 4**
8. n+ implant phosphorus dose=$3x10^{15}$ cm^{-2} energy=50 keV
9. p+ PE **PE 5**
10. p+ implant boron dose=$3x10^{15}$ cm^{-2} energy=20 keV
11. Source/drain implant anneal T=950°C time=5 min N_2

D. Contacts and Metallization **PE 6, PE7**

Using the information given in the process description, answer the following questions.

a) Estimate the sheet resistance and junction depth of the p-well. *10 marks*

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b) Estimate the threshold voltage of the nMOS transistor. *15 marks*

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Cross-Section:

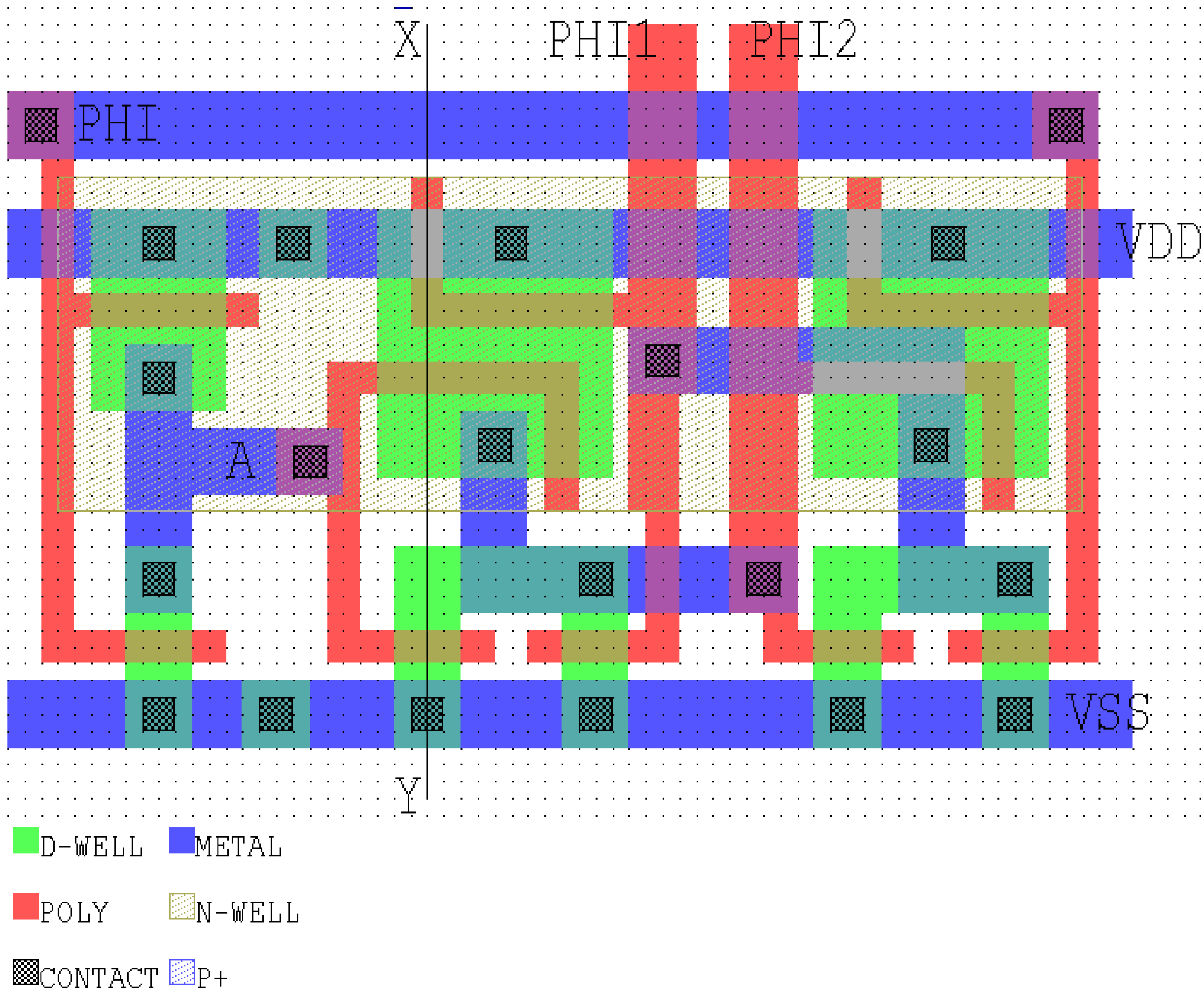

Fig. 1.1

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Equations and Constants

Physical constants: $q = 1.6\text{x}10^{-19}$ C $k = 1.38\text{x}10^{-23}$ JK^{-1} $\varepsilon_0 = 8.85\text{x}10^{-12}$ Fm^{-1} = $8.85\text{x}10^{-14}$ Fcm^{-1}
1eV = $1.6\text{x}10^{-19}$ J $kT/q = 0.0259$ V at room temperature 0°C = 273K

Data for silicon at 300K: $n_i = 10^{10}$ cm^{-3} $E_G = 1.12$ eV $N_C = 2.8\text{x}10^{19}$ cm^{-3} $N_V = 1\text{x}10^{19}$ cm^{-3}
$\varepsilon_s = 11.9\varepsilon_0$ $\mu_n = 1350$ cm^{2}V^{-1}s^{-1} $\mu_p = 480$ cm^{2}V^{-1}s^{-1} $\varepsilon_{ox} = 3.9\varepsilon_0$
in lightly doped material $\mu_n = 1350$ cm^{2}V^{-1}s^{-1} $\mu_p = 480$ cm^{2}V^{-1}s^{-1}

nMOS threshold voltage: $V_{Tn} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_A}{n_i})$ and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

pMOS threshold voltage: $V_{Tp} = V_{FB} - 2\phi_B - \frac{\sqrt{2\varepsilon_s q N_D (2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_D}{n_i})$

Resistivity: $\rho = \frac{1}{q\mu N}$

Saturation drain current: $I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_T)^2}{2}$

Triode drain current: $I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$

In the following Q_{impl} is the implanted dopant dose (ions/cm^2):

Drive-in diffusion profile: $C(x) = \frac{Q_{impl}}{\sqrt{\pi D t}} e^{-x^2/(4Dt)}$

Ion implant profile: $C(x) = \frac{Q_{impl}}{\sqrt{2\pi}\,\Delta R_P} e^{-(x-R_P)^2/(2\Delta R_P^2)}$

Sheet resistance: $R_S \approx \frac{1}{q\mu Q_{impl}}$

Diffusion coefficient: $D = D_0 e^{-E_A/kT}$ ("Intrinsic" diffusion coefficient for lightly-doped material)

Boron: $D_0 = 1.0$ cm^{2}s^{-1} $E_A = 3.5$ eV Phosphorus: $D_0 = 4.7$ cm^{2}s^{-1} $E_A = 3.68$ eV

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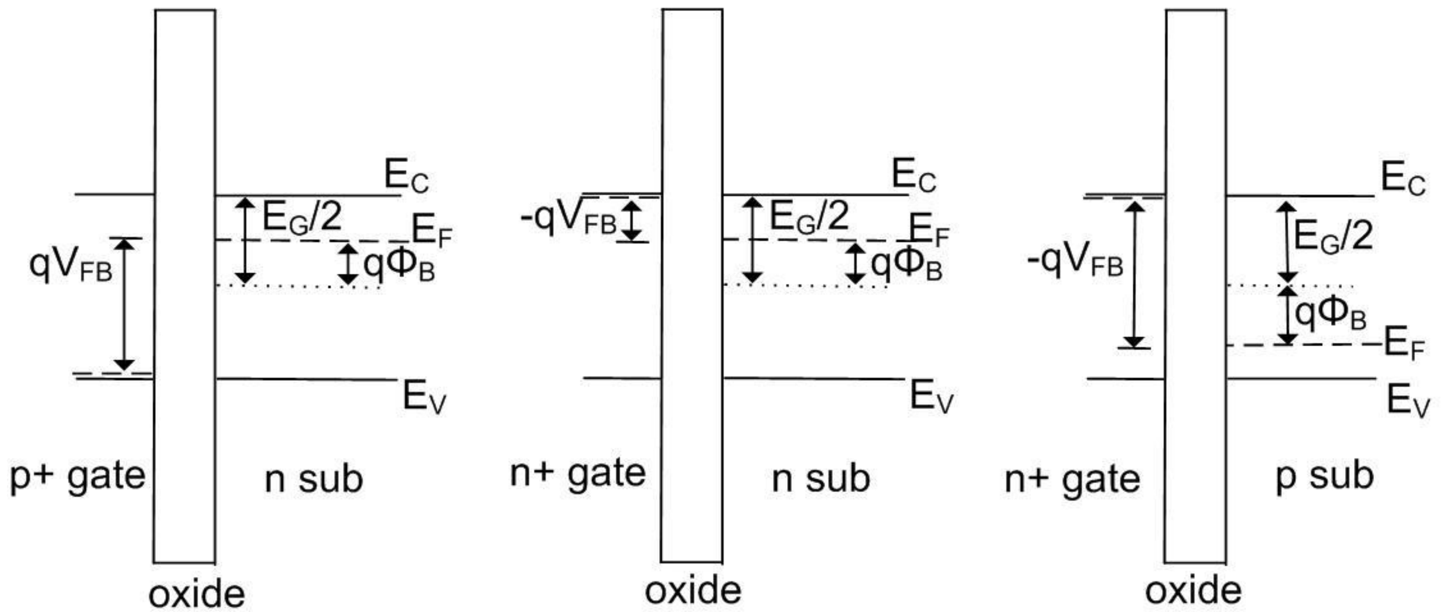
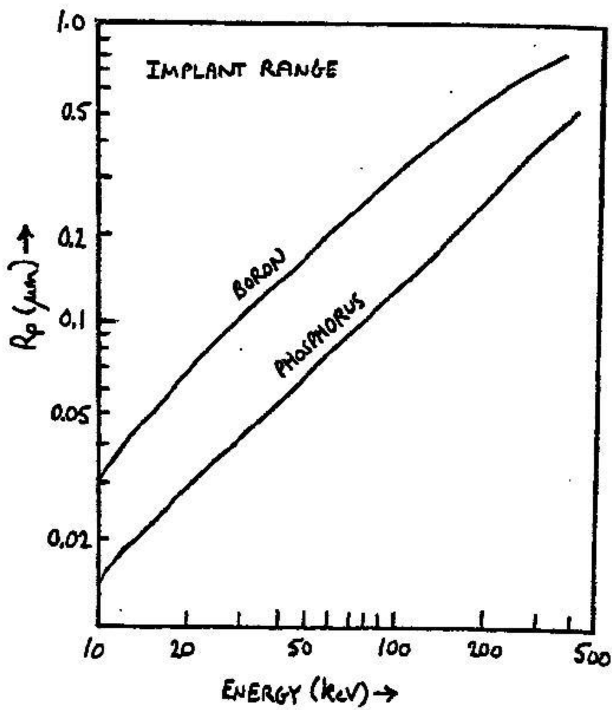
Graphical Data



Diagrams for V_{FB} calculation



Implant range and straggle
(assume straggle is equal to range: $\Delta R_P = R_P$)