Solutions

Name: ______________________ Student Number: __________

CARLETON UNIVERSITY

FINAL EXAMINATION April 2012

DURATION: 3 **HOURS** **Number of Students:** 26

Department Name & Course Number: ELEC 4609 Section A

Course Instructors: N.G. Tarr

Authorized Memoranda: Non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has ten (10) pages.

This examination question paper **may not** be taken from the examination room.

In addition to this question paper, students require: an examination booklet yes ☐ no ☒
a Scantron sheet yes ☐ no ☒

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

SEE LAST TWO PAGES OF EXAM FOR DATA AND FORMULAS

WRITE YOUR NAME AND STUDENT NUMBER ON EACH PAGE

Question	Mark
1	
2	
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Total	

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1. Fig. 1.1 on p. 8 shows the layout of a circuit fabricated in the n-well CMOS technology used in Lab 2. The layout is not complete: the p+ mask is not shown. Draw the outline of this region (or regions) on the layout, and use cross-hatching to indicate the interior of the region. (*Note*: In this CMOS technology, by default any region which is not covered by the p+ layer receives the n+ implant) *4 marks*

2. In the space provided below the layout in Fig. 1.1, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *16 marks*

3. a) Underneath the layout of Fig. 1.1, draw the circuit schematic corresponding to the layout. Show the substrate (body) connection for each transistor. *10 marks*

   b) On the circuit schematic, indicate which transistor(s) may have their threshold voltages modified by the body effect. *3 marks*

   c) Determine the W/L ratio for each transistor and write it on the circuit schematic. *3 marks*

   d) Complete the timing diagram in Fig. 3.1 below showing the output waveform Q produced by the circuit. "T" is short for "Toggle". Briefly explain your answer. 11 *marks*

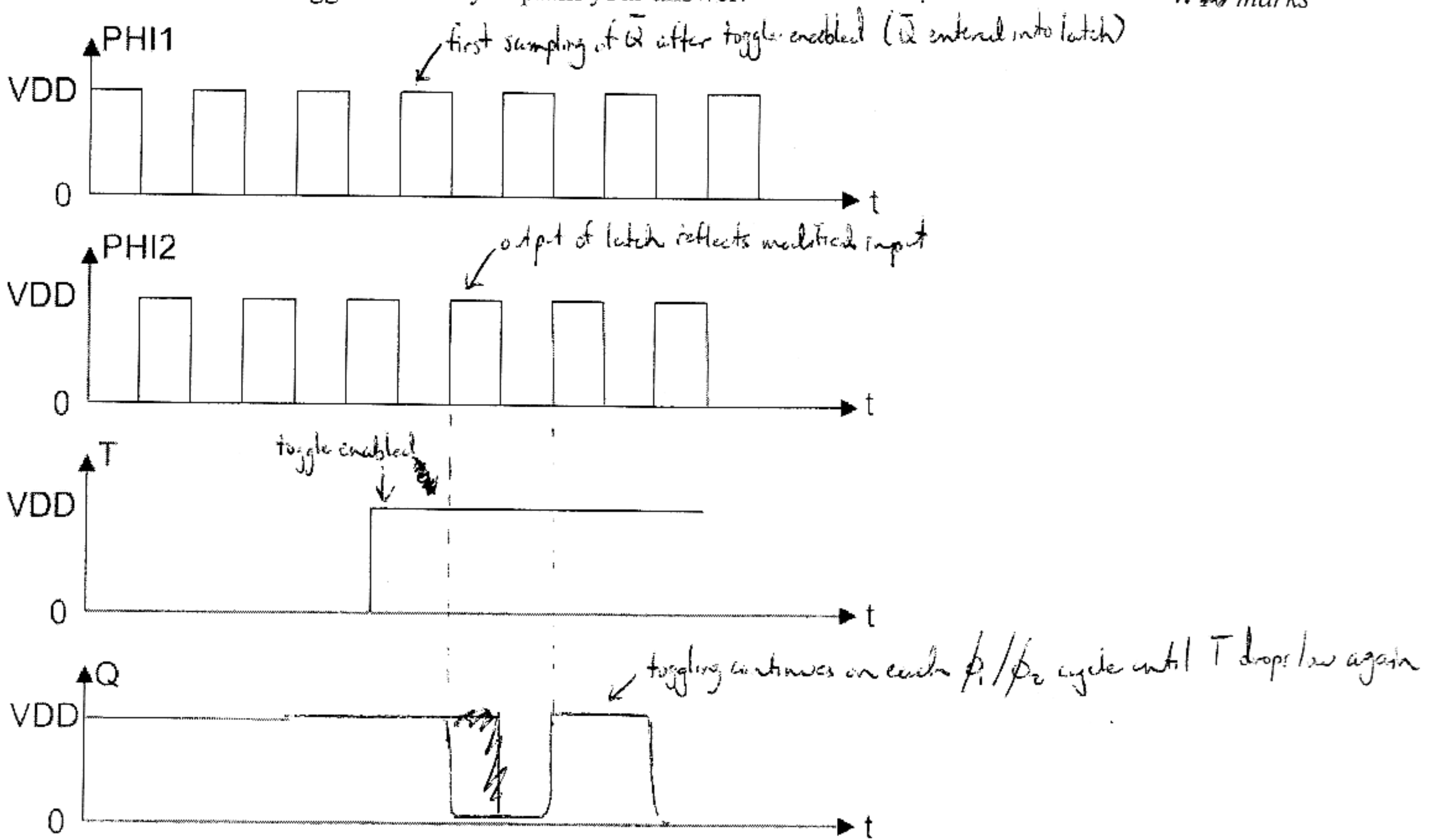

Fig. 3.1

e) Show how your schematic could be modified to provide an asynchronous reset capability that will force Q low when the reset line is high. *3 marks*

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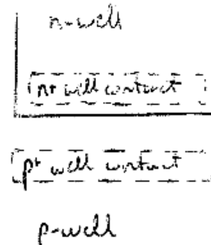
4. The layout of Fig. 1.1 is prone to latch-up. Explain why. Briefly explain how the layout could be modified to minimize the tendency for latch-up. *4 marks*

The n-well and p-well contacts are not close to the well edges.
The contacts should be placed as follows:



5. a) Will the inverter in the circuit of Fig. 1.1 with input labelled "A" give equal output rise and fall times when driven by a square wave input swinging from 0 to V_{DD}? Briefly explain. *marks*

This inverter has $W/L = 2$ for both pMOS pull-up and nMOS pull-down transistors. Since the holes in the pMOS channel have roughly half the mobility of the electrons in the nMOS channel, the rise time will be about twice as long as the fall time.

b) Over what range does the voltage at node A actually swing? Explain briefly. *mark*

The voltage at node A is supplied through an nMOS transmission gate.
The highest it can rise (when the gate of the MOSFET switch is at V_{DD}) is $V_{DD} - V_T$.
Because of this, it is actually reasonable to use equal W/L for the nMOS and pMOS transistors in the inverter.

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6. The circuit of Fig. 6.1 produces a voltage at node Y that is proportional to absolute temperature (PTAT).

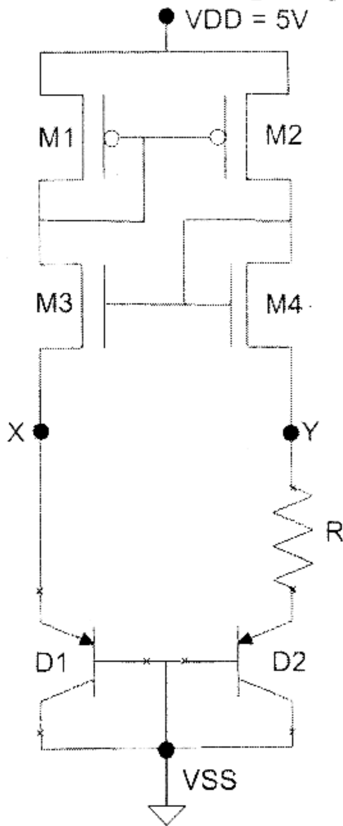

Fig. 6.1 Base-emitter area of D2 is ten times that of D1

a) Assuming transistors M1 and M2 are ideal identical long channel devices operating in saturation, explain why the currents through M1 and M2 are equal. *4 marks*

V_{GS} is the same for M1 and M2. In saturation I_D only depends on V_{GS}, so the currents must be equal

b) Assuming transistors M3 and M4 are identical ideal long channel devices in saturation, explain why the voltage at node X is equal to the voltage at node Y. *4 marks*

From part (a), M3 and M4 must carry the same current I_D. If they are in saturation, this means they must have the same V_{GS} – but the gates are at the same potential so the sources must be too.

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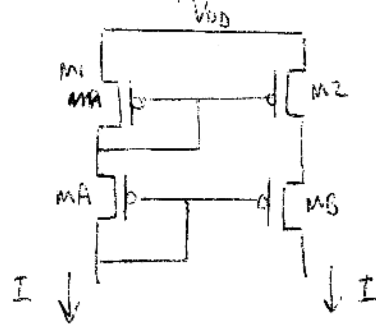
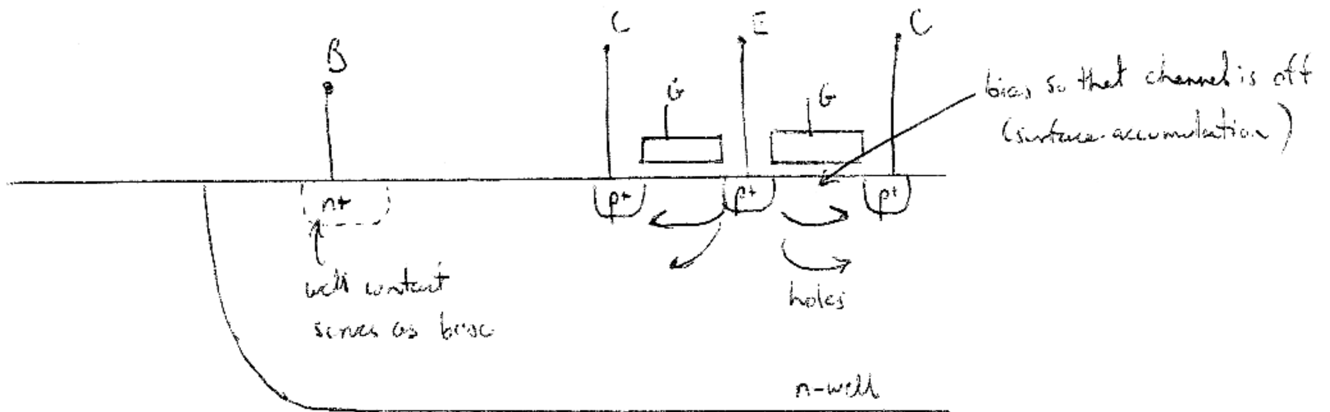
c) Suggest a modification to the circuit that could help keep the current through the left and right branches equal, even if M1 and M2 are not ideal. Draw a schematic for the modification. *4 marks*

Cascode current mirror:



— drains of M1 and M2 at nearly the same potential, which improves current matching.

d) The PTAT circuit requires use of a bipolar transistor. Sketch the structure of a lateral *pnp* bipolar transistor that can be made in a conventional n-well CMOS technology. Explain how the device should be biased to operate as a bipolar transistor. *6 marks*



Bias: CB junction in reverse bias ∴ C negative relative to B

BE junction in forward bias: E positive relative to B

~~Host~~ MOSFET channel turned off: G positive relative to E by at least $|V_{Tp}|$

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7. Fig. 7.1 shows a cross-section through a high voltage MOSFET that could be made in a modified ELEC4609 nMOS process. The device has a lightly doped drain (LDD) region extending from the edge of the gate a distance L_D to a more heavily doped $n+$ drain contact. The gate oxide thickness is 100 nm. The device is formed in a uniformly-doped (100) p-type substrate of 10 Ωcm resistivity. The polysilicon gate is heavily doped with phosphorus.

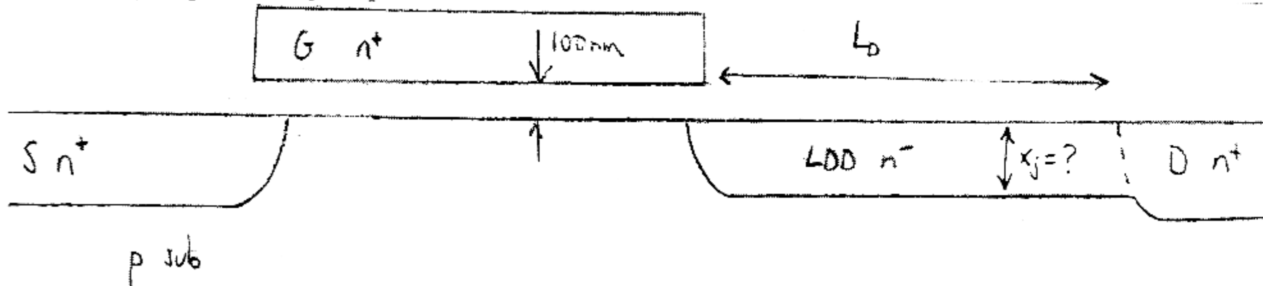

Fig. 7.1

a) If there is no threshold adjust implant, what backgate bias V_{SB} is required to give V_{Tn} = 0.7 V? (Note: the LDD region has no effect on V_T). *14 marks*

$$V_{Tn} = V_{FB} + 2\phi_B + \frac{\sqrt{2\epsilon_s q N_A (2\phi_B + V_{SB})}}{C_{ox}} \qquad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9(8.85\times10^{-14}\,F\,cm^{-1})}{100\times10^{-7}\,cm} = 3.45\times10^{-8}\,F\,cm^{-2}$$

$$\rho = \frac{1}{q\mu_p N_A} \qquad \therefore N_A = \frac{1}{q\mu_p \rho} = \frac{1}{(1.6\times10^{-19})(480\,cm^2V^{-1}s^{-1})(10\,\Omega cm)} = 1.3\times10^{+15}\,cm^{-3}$$

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 0.0259\ln\left(\frac{1.3\times10^{15}}{10^{10}}\right) = 0.305V$$

From band diagram $V_{FB} = -\frac{E_G}{2q} - \phi_B = -\frac{1.12V}{2} - 0.305V = -0.865V$

$$2\epsilon_s q N_A (2\phi_B + V_{SB}) = C_{ox}^2\left[V_{Tn} - V_{FB} - 2\phi_B\right]^2 \qquad \therefore V_{SB} = \frac{\left[C_{ox}(V_{Tn} - V_{FB} - 2\phi_B)\right]^2}{2\epsilon_s q N_A} - 2\phi_B$$

$$V_{SB} = \frac{\left[(3.45\times10^{-8})(0.7 + 0.865 - 0.610)\right]^2}{2(11.9)(8.85\times10^{-14})(1.6\times10^{-19})(1.3\times10^{15})} - 0.610 = 1.86V$$

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b) The LDD region is formed using a phosphorus implant with an energy of 20 keV and a dose of 3×10^{13} cm^{-2} followed by a drive-in diffusion at 1100°C for 10 minutes. All oxide is removed from the silicon surface prior to the implant. What is the metallurgical junction depth x_j for the n- LDD region? Show your work and state any assumptions made. *9 marks*

Assume the profile is determined primarily by diffusion, so $C(x) = \frac{Q_{impl}}{\sqrt{\pi D t}} e^{-x^2/4Dt}$

At the metallurgical junction $C(x) = N_A$ $\therefore \frac{Q_{impl}}{\sqrt{\pi D t}} e^{-x_j^2/4Dt} = N_A$ $e^{-x_j^2/4Dt} = \frac{\sqrt{\pi D t}\, N_A}{Q_{impl}}$

$$x_j = 2\sqrt{Dt}\left[\ln\left(\frac{Q_{impl}}{\sqrt{\pi D t}\, N_A}\right)\right]^{1/2}$$

from diffusion chart at 1100°C $D \simeq 10^{-13}$ cm^2 s^{-1}

$$\sqrt{Dt} = \sqrt{(10^{-13})(600)} = 7.75 \times 10^{-6} \text{ cm}$$

$$\therefore x_j = 2(7.75\times10^{-6})\left[\ln\left(\frac{3\times10^{13}}{\sqrt{\pi}(7.75\times10^{-6})\,1.03\times10^{15}}\right)\right]^{1/2} = 4.29\times10^{-5} \text{ cm} = 0.0429\ \mu\text{m}$$

c) Estimate the sheet resistance of the LDD region. *2 marks*

$$R_s \simeq \frac{1}{q\mu_n Q_{impl}} = \frac{1}{(1.6\times10^{-19})(1350 \text{ cm}^2 V^{-1} s^{-1})(3\times10^{13} \text{ cm}^{-2})} = 154\ \Omega/\square$$

↑ underestimate since μ_n is smaller than this

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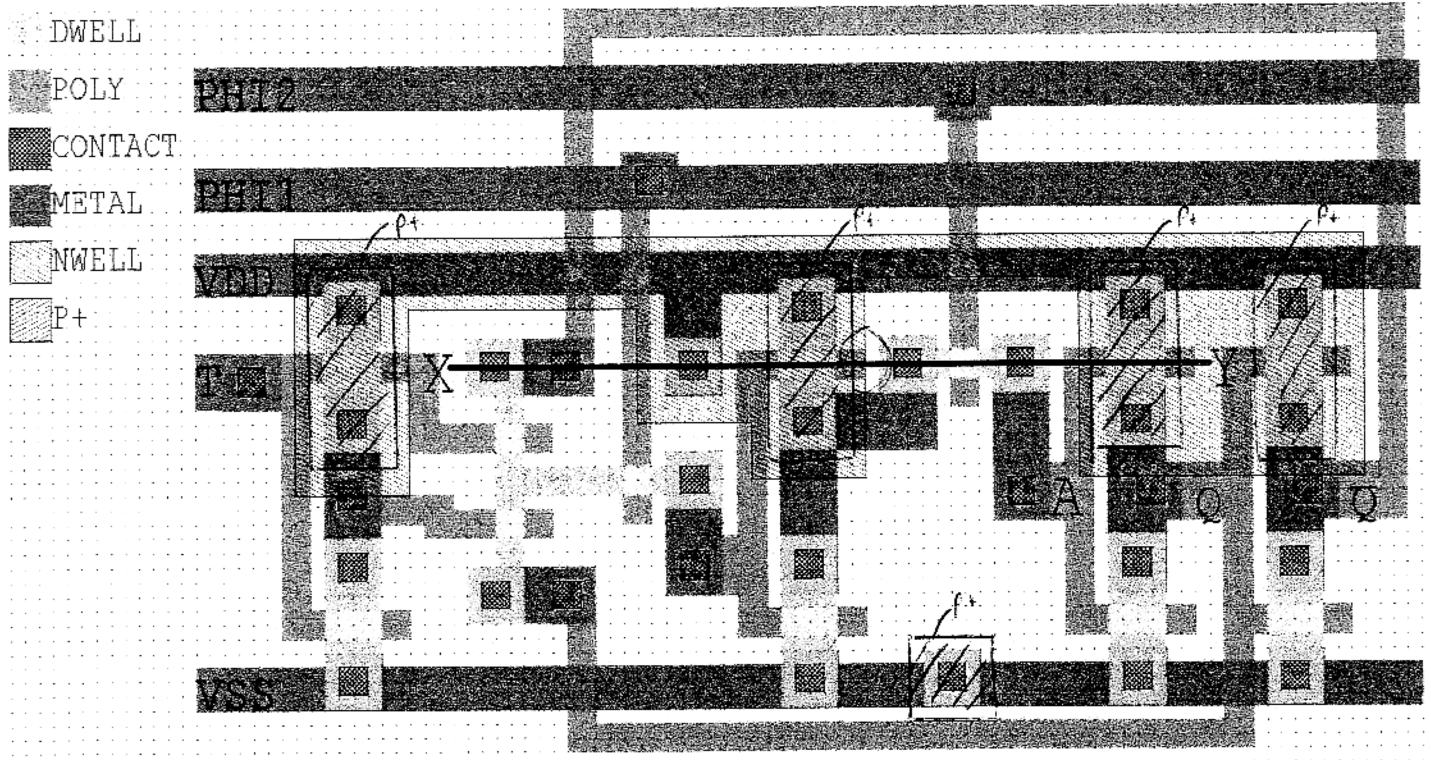

Fig. 1.1