Name: _____ Student Number: _____

CARLETON UNIVERSITY

FINAL EXAMINATION December 2006

DURATION: 3 **HOURS** **No. of Students:** 60

Department Name & Course Number: Electronics ELEC 4609 A

Course Instructor: N.G. Tarr

Authorized memoranda: non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has nine (9) pages.

This examination question paper **may not** be taken from the examination room.

In addition to this question paper, students require: an examination booklet yes ☐ no ☒
a Scantron sheet yes ☐ no ☒

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

Physical constants: $q = 1.6\times10^{-19}$ C $k = 1.38\times10^{-23}$ JK^{-1} $\epsilon_0 = 8.85\times10^{-12}$ Fm^{-1} $= 8.85\times10^{-14}$ Fcm^{-1}
$1eV = 1.6\times10^{-19}$ J $kT/q = 0.0259$ V

Data for silicon at 300K: $n_i = 10^{10}$ cm^{-3} $E_G = 1.12$ eV $N_C = 2.8\times10^{19}$ cm^{-3} $N_V = 1\times10^{19}$ cm^{-3}
$\epsilon_s = 11.9\epsilon_0$ $\mu_n = 1350$ cm^{2}V^{-1}s^{-1} $\mu_p = 480$ cm^{2}V^{-1}s^{-1} $\epsilon_{ox} = 3.9\epsilon_0$

MOSFET threshold voltage:

$$V_{Tn} = V_{FB} + 2\phi_b + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_b)}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}} \qquad \phi_b = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$V_{Tp} = V_{FB} - 2\phi_b - \frac{\sqrt{2\varepsilon_s q N_D (2\phi_b)}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}} \qquad \phi_b = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right)$$

nMOSFET saturation drain current ($V_{DS} > V_{GS} - V_T$):

$$I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_T)^2}{2}$$

nMOSFET triode drain current ($V_{DS} < V_{GS} - V_T$):

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

Additional equations and data on p.8

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1. Fig. 1.1 on p. 9 shows the layout of a circuit fabricated in the n-well CMOS technology used in Lab 2. This circuit uses the 2-phase dynamic logic approach of the 4609 project modified for CMOS; ϕ_1 and ϕ_2 are 2-phase non-overlapping clocks. The layout is not complete: the p+ regions are not shown. Draw the outline of these regions on the layout, and use cross-hatching to indicate the interior of the regions. (*Note*: In this CMOS technology, by default any region which is not covered by the p+ layer receives the n+ implant). *4 marks*

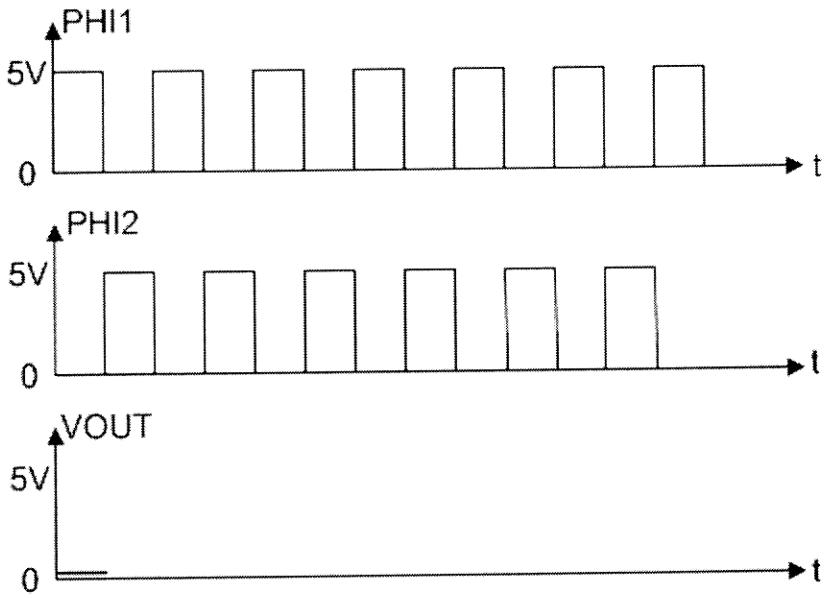
2. In the space provided to the right of the layout in Fig. 1.1, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *16 marks*

3. a) Underneath the layout of Fig. 1.1, draw the circuit schematic corresponding to the layout. Show the substrate (body) connection for each transistor. *7 marks*

   b) On the circuit schematic, indicate which transistor(s) may have their threshold voltages modified by the body effect. *2 marks*

   c) Determine the W/L ratio for each transistor and write it on the circuit schematic. *1 mark*

   d) Complete the timing diagram below showing the output waveform produced by the circuit. Briefly explain your answer. *8 marks*



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e) The circuit of Fig. 1.1 does not take full advantage of the ability of CMOS technology to provide zero power dissipation as the clock frequency approaches zero. In the space below redraw the circuit schematic to correct this deficiency. Also revise the circuit to give equal output rise and fall times. Briefly explain the changes you have made. Assume $\mu_n = 2\mu_p$. *10 marks*

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4. a) MOS integrated circuits are prone to damage from electrostatic discharge (ESD). Briefly explain why.
2 marks

b) Draw the schematic for a circuit which could be connected to a bond pad in CMOS to provide protection against ESD. Your structure should protect against both positive and negative input swings. Briefly explain how your ESD protection structure works.
5 marks

c) Make a rough sketch of the layout of your circuit from part (b) above. Latch-up is often initiated from I/O pads, so make your layout latch up immune. Briefly explain the steps you have taken to maximize latch-up immunity.
5 marks

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5. A basic DRAM sense amplifier circuit is shown in Fig. 5.1. The inverter is driven by an ideal pulse generator with infinitely short rise and fall times. For the sense amplifier to work properly, when $\overline{\text{LATCH}}$ switches low the voltage V_A must rise slowly. Estimate the ratios $(W/L)_{pu}$ and $(W/L)_{pd}$ required to satisfy the following conditions:

   i) slew rate $dV_A/dt = 10^8$ Vs^{-1} when $V_A = 1$ V and $\overline{\text{LATCH}}$ is zero, and

   ii) steady state $V_A = 0.2$ V when $\overline{\text{LATCH}}$ has been high (5 V) for a long time.

   The circuit is designed in Carleton nMOS with $V_{Tn} = 0.7$ V, $\mu_n = 600$ $cm^2V^{-1}s^{-1}$, and $t_{ox} = 50$ nm. $V_{DD} = 5$ V. Ignore the body effect in your calculations. Qualitatively, how would including the body effect alter your answer? *16 marks*

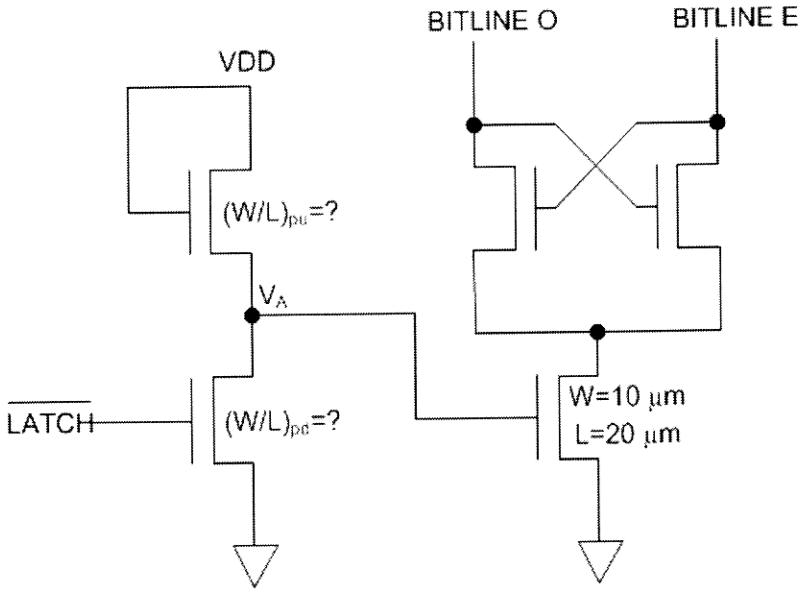

Fig. 5.1 Simple sense amplifier

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6. A possible process flow summary for the n-well CMOS technology of Lab 3 is given below.

Simple 5 μm n-well CMOS Process Flow Outline

Starting material: 6 Ω cm p-type (100) orientation

A. N- well formation

1. First mask oxidation t_{ox} = 200 nm T = 1000°C time = 30 min wet O_2
2. N-well P.E. and oxide etch — PE 1
3. N-well implant phosphorus dose = 2.2×10^{12} cm^{-2} energy = 30 keV
4. Well drive-in T=1100°C time = 16 hours ambient: dilute O_2 in Ar

B. Device Isolation

1. Blanket oxide etchback
2. Pad oxidation t_{ox}=50 nm T=1000°C time = 1 hour dry O_2
3. Nitride deposition $t_{nitride}$= 80 nm
4. Device well P.E. and nitride etch — PE 2
5. p-guard P.E. — PE 3
6. p-guard implant dose = 1×10^{13} cm^{-2} energy = 30 keV
7. Field oxidation t_{ox}=1 μm T=1000°C time= 5 hours wet O_2

C. Active device formation

1. Blanket nitride and pad oxide etchback
2. Gate oxidation t_{ox} = 50 nm T=1000°C time = 1 hour dry O_2
3. Blanket active device V_T adjust implant boron dose = 4×10^{11} cm^{-2} energy = 30 keV
4. Gate polysilicon deposition t_{poly} = 0.4 μm
5. Blanket poly doping phosphorus (solid solubility chemical source) T=1000°C
6. Polysilicon gate P.E. and etch — PE 4
7. Gate oxide etchback
8. n+ PE — PE 5
9. n+ implant phosphorus dose = 3×10^{15} cm^{-2} energy = 50 keV
10. p+ PE — PE 6
11. p+ implant boron dose = 3×10^{15} cm^{-2} energy = 20 keV
12. Source/drain implant anneal T = 1000°C time = 10 min ambient = N_2

D.Contact and Metallization

1. BPSG deposition
2. BPSG flow
3. Contact P.E. and etch — PE 7
4. Metal deposition
5. Metal P.E. and etch — PE 8

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a) Selecting the relevant information from the process flow above, compute the field threshold voltage $V_{Tp,field}$ of the parasitic transistor formed by polysilicon crossing field oxide over the n-well. Show your calculations and state any significant approximations made in them. *18 marks*

b) Estimate the junction depth and sheet resistance of the n-well. State any approximations made in your calculation *6 marks*

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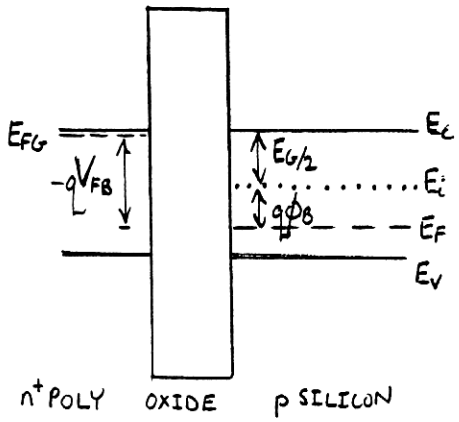
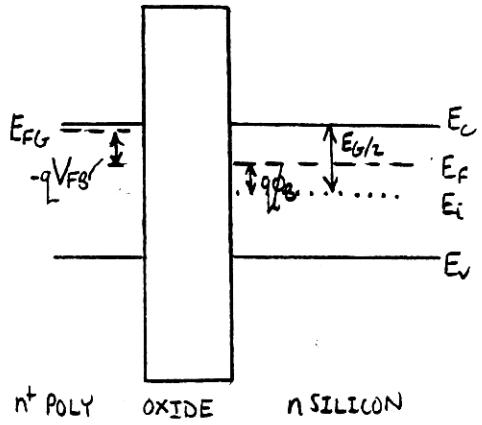
Resistivity: $\rho = \dfrac{1}{q\mu N}$

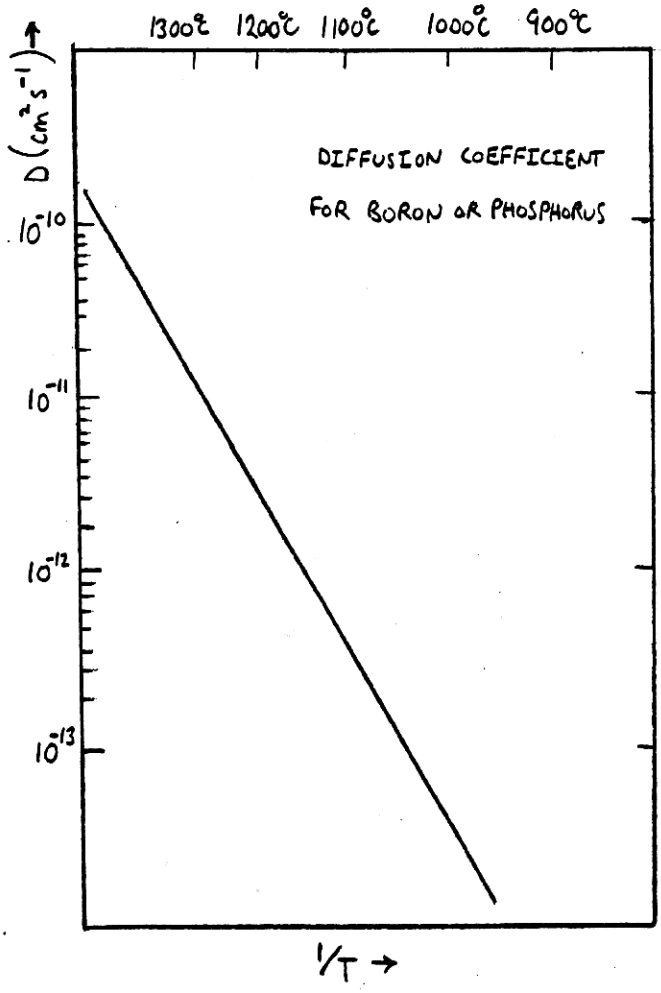
ion implant: $C(x) = \dfrac{Q}{\sqrt{2\pi}\,\Delta R_p} \exp\left(\dfrac{-(x-R_p)^2}{2\Delta R_p^2}\right)$

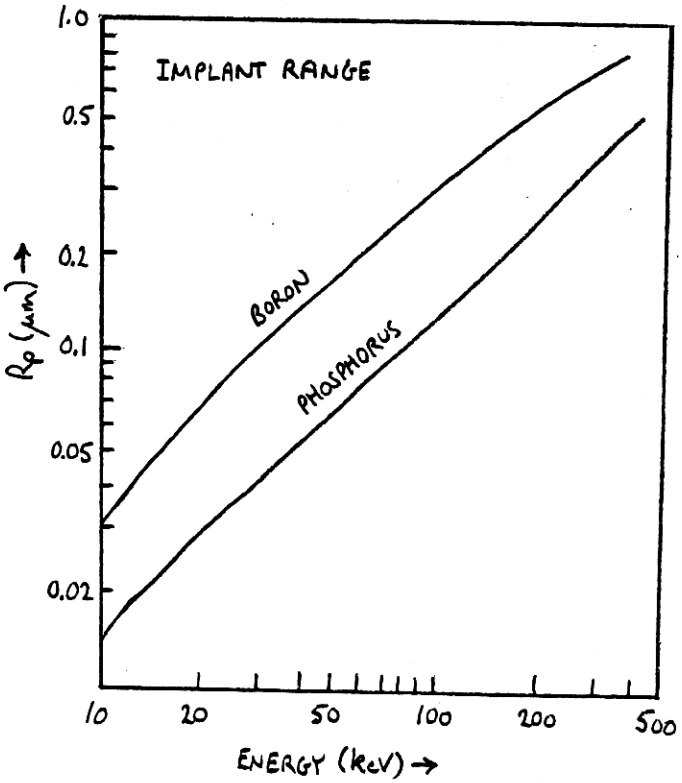
drive-in: $C(x) = \dfrac{Q}{\sqrt{\pi D t}} \exp\left(\dfrac{-x^2}{4Dt}\right)$

sheet resistance: $R_s = \dfrac{1}{q\int_0^{x_j} \mu\,(C(x)-C_B)\,dx} \approx \dfrac{1}{q\overline{\mu}\,Q}$









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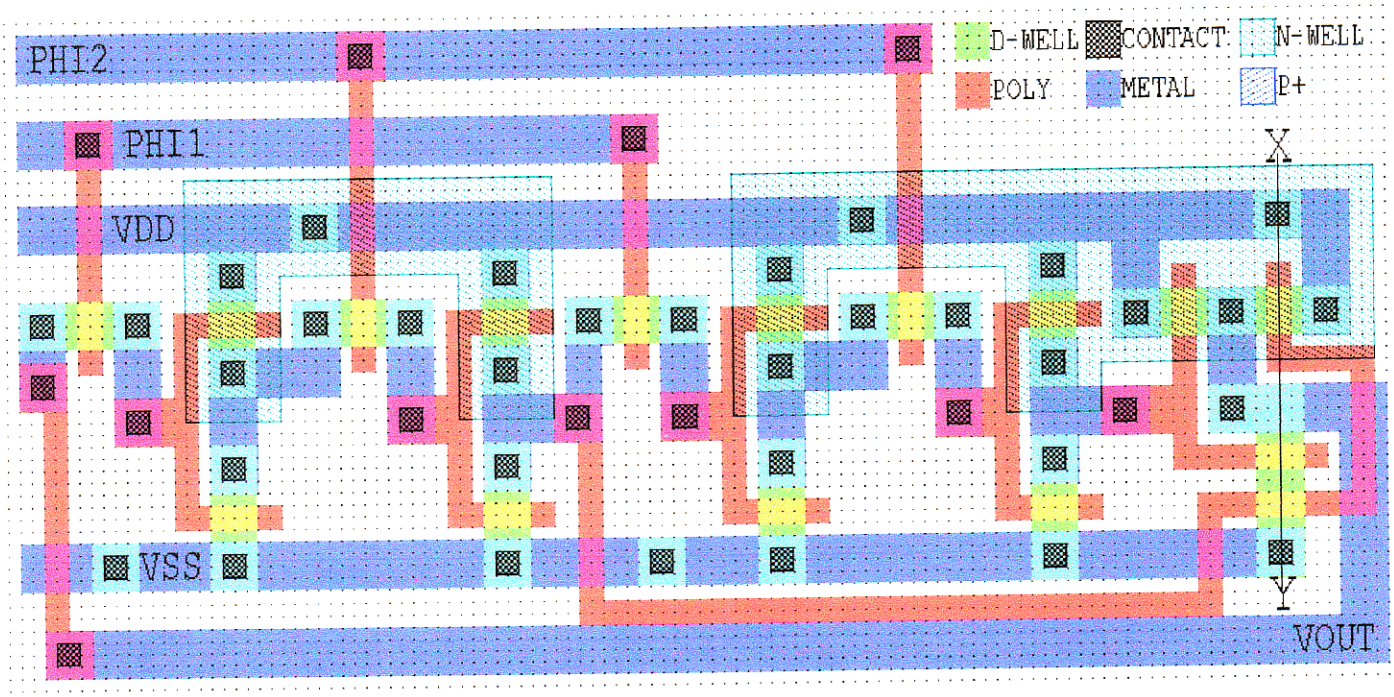

Fig. 1.1 CMOS layout for questions 1, 2, and 3.