ELEC 4609 **IC DESIGN DIGITAL PROJECT REPORT GUIDELINES** Winter 2017

A comprehensive and complete but concise report on the ELEC 4609 IC design project is expected. Write your report in a similar order to the guidelines below. Write a complete report containing the information specified in the guidelines. **Do not simply answer the questions like you would on an assignment!** It might help to imagine that you completed the project design in industry, and are now writing a report on your work for your employer. Your employer is familiar with CMOS design and doesn't want a lot of background. Before paying to fabricate your design your employer **does** want evidence that it has been fully verified with all available CAD tools, and so is likely to work. Your employer would also like some justification that your design is making efficient use of expensive silicon real estate. Finally, if it becomes necessary to modify your design at some future time, your employer wants a report that another experienced engineer can use to quickly understand the design and determine where modifications are to be made.

Late submissions will be penalized. Any changes to this will be posted on the course website.

Submissions should be made via CuLearn. The file name should be in the following format: first initial, last initial, student number. For example: John Doe would be jd100XXXXXX.pdf

If your layout did not LVS clean before fabrication submission, you must submit your now LVS clean layout and schematic in a zip folder.

Although in most cases the design work was done in groups of two, individual reports are expected from the group members. Reports should identify how the work of the group was divided.

The guidelines below assume that you completed the "baseline" digital project. If you completed an alternative project you may need to modify the report appropriately.

If you have improved your design since the February submission deadline, you may report on the improved design rather than the original. However, you should include the original design as an appendix to the report, along with a brief description of the improvements made.

Discuss all images in the body of your report!

Detailed Guidelines:

1. Introduction: Design overview with specifications.

2. System level block diagram of the complete project with a discussion on the functionality of each block (high level block diagram should contain only flip-flops, XNOR, master clock generator, 2-phase clock generator and output buffer).

3. Design of the individual blocks:

a) INV:
- Include circuit schematics with W and L clearly labeled for each MOSFET
- Truth table showing the predicted sequence
- Show an example layout of an INV from your final layout, labeling all ports and removing all other devices from the image

b) NAND:
- Include circuit schematics with W and L clearly labeled for each MOSFET
- Truth table showing the predicted sequence
- Show an example layout of a NAND from your final layout, labeling all ports and removing all other devices from the image

c) NOR:
- Include circuit schematics with W and L clearly labeled for each MOSFET
- Truth table showing the predicted sequence

- Show the layout of the NOR from your final layout, labeling all ports and removing all other devices from the image

d) XNOR:
   - Include circuit schematics with W and L clearly labeled for each MOSFET
   - Truth table showing the predicted sequence
   - Show the layout of the XNOR from your final layout, labeling all ports and removing all other devices from the image
e) Master Clock Generator:
   - Include circuit schematics with W and L clearly labeled for each MOSFET
   - Include a clearly labeled SPICE simulation plot of the master clock waveform
   - Show the layout of the Master Clock Generator from your final layout, labeling all ports and removing all other devices from the image
f) 2-Phase Clock Generator:
   - Include circuit schematics with W and L clearly labeled for each MOSFET
   - Include a clearly labeled SPICE simulation plot of each 2-phase clock waveforms
   - Include a clearly labeled SPICE simulation plot of the overlap between the 2-phase clock waveforms. Explain the importance of minimizing overlap.
   - Show the layout of the 2-Phase Clock Generator from your final layout, labeling all ports and removing all other devices from the image
g) D Flip-Flop:
   - Include circuit schematics with W and L clearly labeled for each MOSFET
   - Identify the type of MOSFET used for the transmission gates, highlighting the benefits and disadvantages.
   - Show the layout of the D Flip-Flop from your final layout, labeling all ports and removing all other devices from the image
h) Output Buffer:
   - Calculations and discussion for MOSFET sizing (W and L)
   - Include circuit schematics with W and L clearly labeled
   - Show the layout of the Output Buffer from your final layout, labeling all ports and removing all other devices from the image
i) Additional Block Types (some groups have different types of blocks, the weight of the marks will be adjusted to balance additional block types):
   - Include circuit schematics with W and L clearly labeled for each MOSFET
   - Truth table showing the predicted sequence (if applicable)
   - Show an example layout of each of your different additional block types from your final layout, labeling all signals and removing all other devices from each image

4. Top level block discussion:

a) Top level schematic (schematic should contain only the PRSG, capacitor, LED with model, and any required voltages sources and grounds)
b) Schematic of complete circuit (schematic should contain with models shift register chain, XNOR, master clock generator, 2-phase clock generator and output buffer)
c) Include a clearly labeled SPICE simulation plot (at least two full cycles) of the PRSG's output
d) Include a clearly labeled long (at least two full cycles) SPICE simulation plot of the PRSG's output with a Reset signal. The reset needs to occur approximately half way through the simulation to show that the reset is properly working. Ensure that the reset is held for a significant period of time to verify that the PRSG has reset.
e) Include a color image of your final layout
f) Show an example layout of an input protection device from your final layout, labeling all ports and removing all other devices from the image
g) Refer to the DRC results of your final layout in the body of your report. Put the DRC results in your Appendix. (remove art work from your DRC check)
h) Refer to the LVS results of your **full, complete final layout** in the body of your report. Put the LVS results in your Appendix. (You may remove input protection from your LVS check)
i) Include a clearly labeled SPICE simulation plot (at least two full cycles) showing the waveform produced by the circuit extracted from the **full, complete final layout.**

j) Comment on any differences between the schematic and extracted PRSG's outputs.
k) Briefly discuss steps you have taken to minimize layout area.

5. Maker's Discretion:

- Proper English
- Clear discussions
- Clear and logical formatting of report
- Plots well labeled
- Schematics are clear and organized
- Present a design report