ELEC 4609 **IC DESIGN ANALOG PROJECT REPORT GUIDELINES** Winter 2017

A comprehensive and complete but concise report on the ELEC 4609 IC design project is expected. Write your report in a similar order to the guidelines below. Write a complete report containing the information specified in the guidelines. **Do not simply answer the questions like you would on an assignment!** It might help to imagine that you completed the project design in industry, and are now writing a report on your work for your employer. Your employer is familiar with CMOS design and doesn't want a lot of background. Before paying to fabricate your design your employer **does** want evidence that it has been fully verified with all available CAD tools, and so is likely to work. Your employer would also like some justification that your design is making efficient use of expensive silicon real estate. Finally, if it becomes necessary to modify your design at some future time, your employer wants a report that another experienced engineer can use to quickly understand the design and determine where modifications are to be made.

Late submissions will be penalized. Any changes to this will be posted on the course website.

Submissions should be made via CuLearn. The file name should be in the following format: first initial, last initial, student number. For example: John Doe would be jd100XXXXXX.pdf

If your layout did not LVS clean before fabrication submission, you must submit your now LVS clean layout and schematic in a zip folder.

Although in most cases the design work was done in groups of two, individual reports are expected from the group members. Reports should identify how the work of the group was divided.

The guidelines below assume that you completed the analog op-amp project.

If you have improved your design since the February submission deadline, you may report on the improved design rather than the original. However, you should include the original design as an appendix to the report, along with a brief description of the improvements made.

Discuss all images in the body of your report!

Detailed Guidelines:

1. Introduction: Design overview with specifications.

2. Biasing Network:
   - Include design calculations for sizing MOSFETs in biasing network
   - Discuss choice of current for biasing network
   - Discuss choice of V_{BIAS}
   - Provide and discuss simulations results of biasing network current and V_{BIAS}

3. Differential Amplifier using Biasing Network:
   - Include design calculations for sizing MOSFETs in differential amplifier
   - Provide and discuss simulations results showing the quiescent voltages at each node of the differential amplifier, DC sweep of the differential amplifier output, DC gain of the differential amplifier, output DC offset of the differential amplifier, and minimum and maximum output voltage of the differential amplifier.

4. Opamp Without Compensation
   - Include design calculations for sizing MOSFETs in gain and output buffer stages
   - Provide and discuss simulations results showing the quiescent voltages at each node of the gain and output buffer stages, DC sweep of the opamp output, DC gain of the opamp, output DC offset of the opamp, and minimum and maximum output voltage of the opamp.

5. Opamp with Compensation
   - Explain why we would want to add frequency compensation to the opamp
   - How can we use a MOSFET as a capacitor?
   - How do we determine if the opamp is stable?
   - Provide and discuss simulations results showing that the opamp is stable. What is the phase margin, 3dB corner frequency, and unity-gain bandwidth of your opamp?

6. Opamp Layout
   - Include a color image of your final layout
   - Discuss any advanced layout techniques in your layout
   - Refer to the DRC results of your final layout in the body of your report. Put the DRC results in your Appendix. (remove art work from your DRC check)
   - Refer to the LVS results of your **full, complete final layout** in the body of your report. Put the LVS results in your Appendix. (You may remove input protection from your LVS check)

5. Maker's Discretion:

   - Proper English
   - Clear discussions
   - Clear and logical formatting of report
   - Plots well labeled
   - Schematics are clear and organized
   - Present a design report