

NOTES ON 2-PHASE NON OVERLAPPING CLOCK GENERATORS

The dynamic shift register used in the baseline ELEC4609 project requires 2-phase non-overlapping clocks. In particular since nMOS transmission gates connect the inverters in the shift register stage, it is important that clocks ϕ_1 and ϕ_2 never be high at the same time. For years we successfully used a generator based on cross-coupled NOR gates as shown in Fig. 1. In this circuit ϕ_2 cannot rise until ϕ_1 has fallen below the switching point for the NOR gate, resulting in the output waveform of Fig. 2.

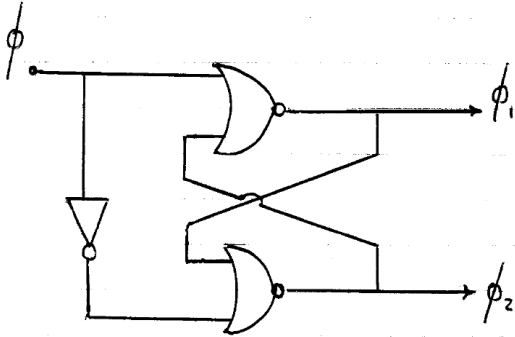


Fig.1

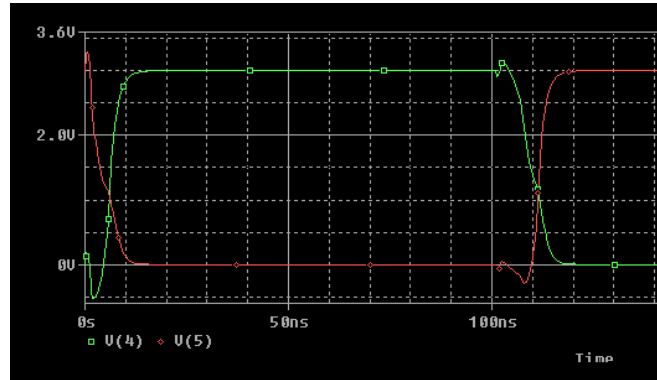


Fig. 2

In CMOS NOR gates take much more area than NAND gates. This suggested switching to a cross-coupled NAND generator as shown in Fig. 3. This circuit is recommended in the Jacob Baker textbook. Unfortunately for this circuit ϕ_1 cannot fall until ϕ_2 has risen, resulting in the output waveform of Fig. 4.

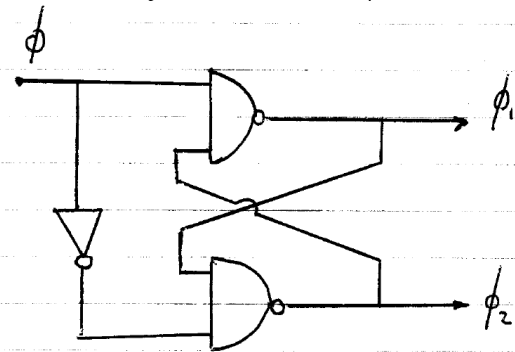


Fig. 3

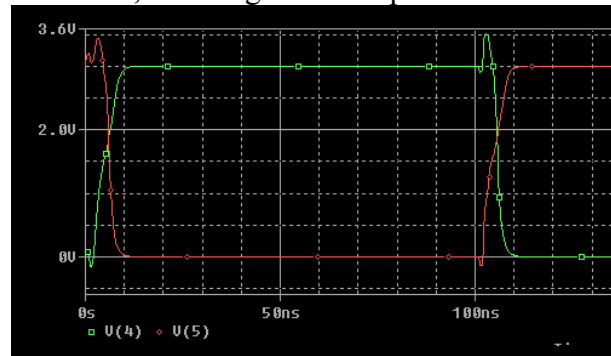


Fig. 4

The overlap interval in which ϕ_1 and ϕ_2 are both above midrail in Fig. 4 is relatively short, so it would probably be possible to use this circuit for 4609. Certainly this circuit would make sense if full CMOS transmission gates were used to connect the inverters in the shift register stage. If you have implemented the cross-coupled NAND generator and SPICE simulation confirms that the complete PRSG works, you are probably safe. However, a better circuit is that shown in Fig. 5. The extra inverters ensure that ϕ_1 and ϕ_2 are never high simultaneously, as confirmed by the SPICE output of Fig. 6. If you are having trouble getting your project to simulate correctly, you might want to consider switching to the Fig. 5 clock generator.

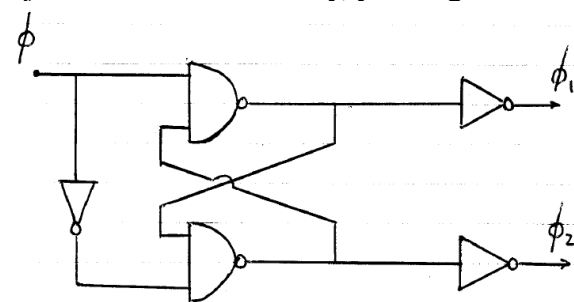


Fig. 5

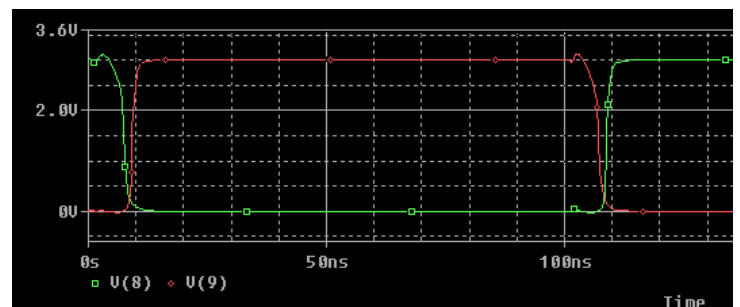


Fig. 6