Lab 4 Simulation Instructions

In this lab, you will again be using the Xilinx ISE to enter the design and simulate it. This is similar to what you were doing in lab 2 and lab 3. Thus, you should review the instructions for lab 2 and lab 3 for precise step by step instructions.

The main difference in lab 4 and the previous labs is that each individual circuit block has its own test bench. This is generally good practice, as it allows you to narrow down problems to specific modules. Thus, it is highly suggested that you enter the design and simulate it one block at a time. To do this, first select the simulation radio button in the Design tab. You will notice a list a test fixture files, each of which corresponds to a single test for one or more modules. For instance, testBitCount.tf is a test fixture for only the "Bit count" module, and testMAJORITY.tf is similarly is a test fixture for only the Majority block. The "test_midi_noisy_top.tf" is a test file for all modules, so only run that when you have finished entering and testing all of your modules and way to test them together.

Note that some of the test benches simulate the operation of the entire circuit by with blocks that emulate the other parts of the circuit that you are not testing. Thus, in order to understand the simulation results, you should try to familiarize yourself with the operation of the entire circuit.

In the second part of lab 4, you will be implementing your design on the CPLD. You can use the same instructions for lab 3 here.