

## **Books:**

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2. Michel Nakhla and Qi-jun Zhang (Editors), *Modelling and Simulation of high-Speed VLSI Interconnects*, Boston, MA: Kluwer Academic Publisher, 1994.

## **Chapters in Books**

1. B. Nouri, E. Gad, M. Nakhla and R. Achar, Model-Order Reduction in Microelectronics, in “Model Order Reduction: Theory, Research Aspects and Applications”, Springer, 2019 (in Press).
2. E. Gad, M. Nakhla and R. Achar, Model-Order Reduction of High-Speed Interconnects using Integrated Congruence Transform, Chapter 17 in “Model Order Reduction: Theory, Research Aspects and Applications”, Springer, 2007.
3. M. Nakhla and R. Achar, Recent Advances in Interconnect Modelling and Simulation of High-Speed Interconnects, Chapter VII in “Computational Methods in Large Scale Simulation”, World Scientific Publishing Co., 2005.
4. J. Chinneck, M. Nakhla, and Q.J. Zhang, Computer-Aided Design for Electrical and Computer Engineering, Chapter VI in “Tutorials on Emerging Methodologies and Applications in Operations Research”, Kluwer Academic Press, 2004.
5. M. Nakhla and R. Achar, Interconnect Modelling and Simulation, Chapter XVII in “VLSI Handbook”, CRC Press, 2000.
6. R. Achar and M. Nakhla, Minimum Realization of Reduced-Order Models of High-Speed Interconnect Macromodels, Chapter III in “Signal Propagation on Interconnects”, Kluwer Academic Press, 1998.
7. M. Nakhla, R. Achar and R. Khazaka, Modeling and Simulation of High-Speed VLSI Interconnects, Chapter IV in “Circuits and Systems in the Information Age”, IEEE press, 1997.
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