

A Low Voltage CMOS Multiplier for High Frequency Equalization

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Abstract - This paper describes the design of a low power 1.2V CMOS multiplier for 10 Gbit/s continuous time finite impulse response (FIR) filter. The multiplier is based on a low noise amplifier (LNA) architecture and has variable gain, which is directly controlled by a 5 bit digital word. This direct control removes the need for a digital to analog converter to set the gain of the multiplier. The 5 bit control word allows 32 possible gain settings from a minimum gain of -1 to a maximum gain +1 with linearity errors less than 1%. The gain is achieved by switching in various combinations of binary weighted gain stages. To achieve negative gain, a swap switch is used which reduces the number of gain stages required and also reduces the parasitic load on the summing node. The circuit requires 1.9mA of current and has a post-extracted bandwidth of 7.6 GHz.

I. INTRODUCTION

As signals are transmitted through a medium, such as air or copper, different frequencies tend to propagate at different speeds due to the frequency response of the medium. This results in amplitude and phase variations between the transmitted and received signal, which leads to inter-symbol interference (ISI). ISI has the effect of impeding the receiving circuitry's ability to distinguish between a 1 or a 0 and can result in data errors. This effect is magnified as the transmission frequency or transmission distance is increased and the amplitude and phase errors accumulate and become more significant and detrimental.

To reduce the effect of ISI an equalizer can be used at the receiving end to control the overall pulse shape of the received data [2]. This re-shaping of the data reduces the transmission effect of the medium, which in turn reduces the ISI allowing an increase in data rates or the distance of transmission. As an example, equalizers can increase the data rate in chip-to-chip communication by compensating for the high frequency loss of the connecting copper traces between chips.

There are generally four categories of receiver equalizers for over Gbps data transmissions: passive-component equalizer, active continuous-time equalizer using split-path amplifier, active equalizer using discrete-time FIR filter and active equalizer using continuous-time FIR filter [4].

This paper focuses on a multiplier design for a continuous time FIR filter, as shown in Figure 1.

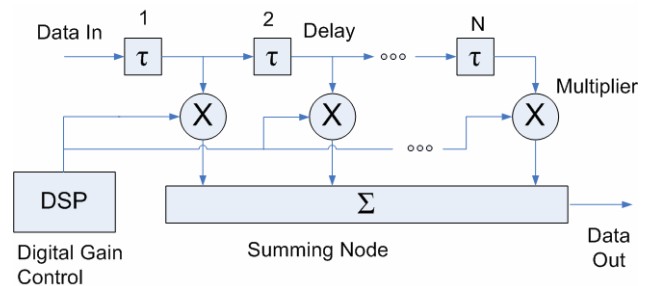


Figure 1. N Tap FIR Filter

Figure 1 represents a N tap FIR transversal filter system where the required number of stages, N, depends on the characteristics of the transmission medium. A medium that introduces large amounts of distortion will require a large number of taps to recover the transmitted signal by reducing the ISI. Ideally an infinite number of taps is required to completely remove all ISI. In practice a large number of taps is not realizable due to the increased capacitive load at the summing node as extra multipliers are added. This capacitive load serves to reduce the bandwidth of the summing node and as the bandwidth falls below the data rate the filter can no longer recover the transmitted signal. Furthermore, as the bandwidth falls below the data rate the FIR filter will low pass filter the received signal, adding extra distortion and increase the ISI. Hence there is a limit to the feasible number of taps. It is the goal of this paper to design a multiplier that is high bandwidth and reduces the capacitance at the summing node, thus allowing more taps and improved recovery from ISI.

II. MULTIPLIER DESIGN

In addition to high bandwidth, the continuous time FIR filter also requires a multiplier that has variable gain and is linear.

Variable gain is achieved through the use of individual gain stages that are switched on or off by the digital control as illustrated in Figure 1. The block level diagram of the multiplier is shown in Figure 2.

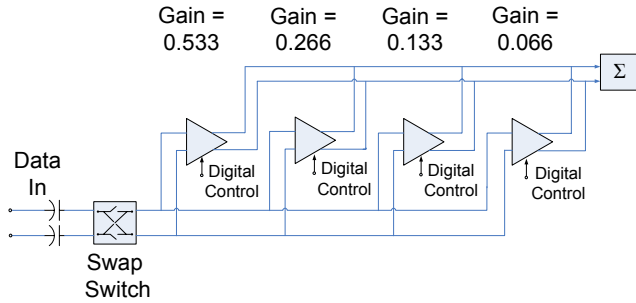


Figure 2. Block diagram of the Multiplier

The gain stages are binary weighted so that various combinations of stages will allow the gain to be increased from a gain of 0 to a maximum gain of 1 with a gain step size of 1/15. Binary weighted current switching requires careful consideration of switching transients and nonlinearity when switching from the binary equivalent of 0111 to 1000.

The negative gain is achieved through the swap switch which is illustrated in Figure 3.

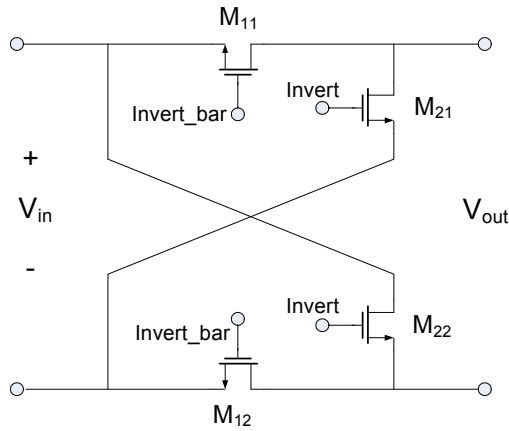


Figure 3. Swap Switch

This switch inverts the input signal by crossing the input wires. This removes the requirement for an extra 4 gain stages with inverted outputs to obtain the negative gain and effectively reduces the potential parasitic loading at the summing node by 50%. The swap switch transistors (M11, M12, M21 and M22) must be large so that their resistance is low enough to prevent the input signal from being attenuated. However, the transistors must not be so large that they present a significant input capacitive load on the driving delay stage, thus limiting the frequency response.

III. MULTIPLIER CIRCUIT IMPLEMENTATION

In an attempt to explore alternative low power/low voltage CMOS multiplier designs, the gain stages were implemented using an LNA architecture as shown in Figure 4.

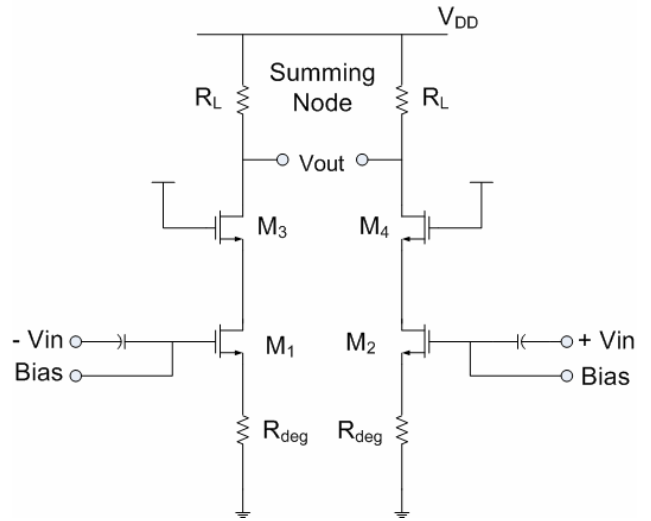


Figure 4. LNA Gain Stage

This specific LNA architecture has the advantage of combining the differential pair and the current source thus reducing the headroom required and making it ideal for low voltage applications.

The sizing of the differential pair transistors (M1 & M2) in Figure 4 is crucial to the operation of the multiplier. As this cell is driven by a delay cell (as illustrated in Figure 1) it is important to keep the input capacitance low and avoid a potential bandwidth bottleneck at the delay multiplier interface. However, the gain of the multiplier pair is roughly proportional to the square root of the width to length ratio (W/L) of the differential pair and the bias current. So to keep the input pair small requires extra current to meet the gain specifications. Thus a careful analysis is required to determine the optimal balance between capacitive input loading, gain, and power. In addition to this, the cascode transistors (M3 & M4) increase the effective bandwidth by reducing the Miller effect. Furthermore, by keeping the cascode transistors smaller than the input transistors (M1 & M2) the parasitic load on the summing node can be minimized.

The gain of each stage is set based on the following gain equation for low noise amplifiers according to [1]:

$$Gain = \frac{g_m R_L}{1 + g_m R_{deg}} \quad (1)$$

When implemented with high g_m transistors, such as bipolar, the denominator can be simplified as follows assuming that $g_m R_{deg} \gg 1$:

$$Gain \cong \frac{g_m R_L}{g_m R_{deg}} \cong \frac{R_L}{R_{deg}} \quad (2)$$

Using CMOS transistors, the achievable g_m is much smaller and the assumption made in (2) does not hold. As a result the gain cannot be set though resistor degeneration alone and both current and the W/L ratio of the differential pair must be varied to obtain the required gains. Thus the gain is no longer determined by a resistor ratio and process variation will have a significant effect on the gain of the multiplier. Given that the multiplier is in a feedback loop controlled by a DSP algorithm, reduced or increased gain will affect the dynamic range, but is acceptable as long as the multiplier remains linear. However, if the multiplier becomes non-linear, or non-monotonic, it is possible that the FIR filter may not stabilize. Thus for such a design, it is important to maintain linearity even with process variations. To facilitate this, each gain stage is a scaled version of the previous stage. All transistors are matched and the number of fingers in transistors M1 & M2, and M3 & M4 are scaled as required. The degeneration resistors in Figure 4, R_{deg} , are also scaled and built from unit resistors that are physically similar. With a proper layout, this leads to a well matched circuit and a very linear multiplier as the different gain stages are switched in.

IV. RESULTS

A single multiplier was simulated with three other multipliers connected to the same summing node to account for the parasitic loading equivalent to a four tap system. Both pre-layout and post-layout simulations were completed. Presently, the chip is being fabricated in a $0.13\mu\text{m}$ CMOS process. The layout of the chip is shown in Figure 5. It occupies an area of $90\mu\text{m}$ by $332\mu\text{m}$.

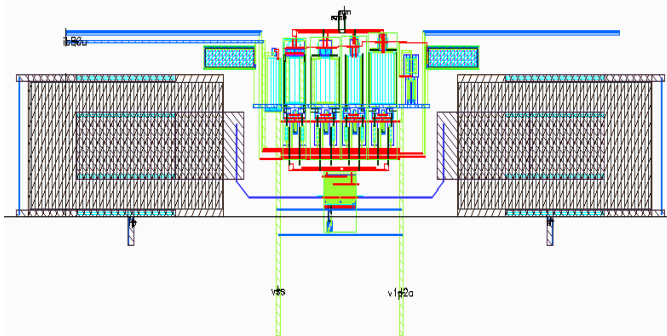


Figure 5. Layout of Multiplier Circuit

The linearity of the multiplier with a input signal swing of 100mV peak differential, digitally stepped though all

positive gains from 0 to a maximum voltage gain of 1 is illustrated in Figure 6

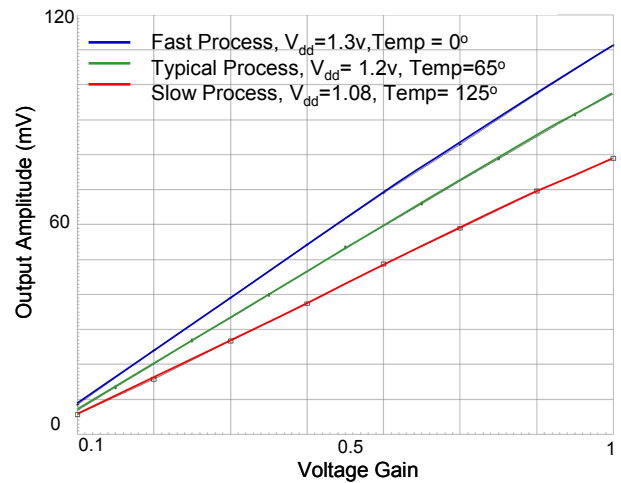


Figure 6. Linearity with Varying Gain Settings

As expected the magnitude of the gain varies with process, temperature, and voltage. Figure 6 also illustrates that even with these variations the multiplier remains linear and monotonic. This linearity must also be present as the signal level of the input varies. Figure 7 illustrates the linearity as the amplitude of the input is swept for both the smallest and largest gain settings.

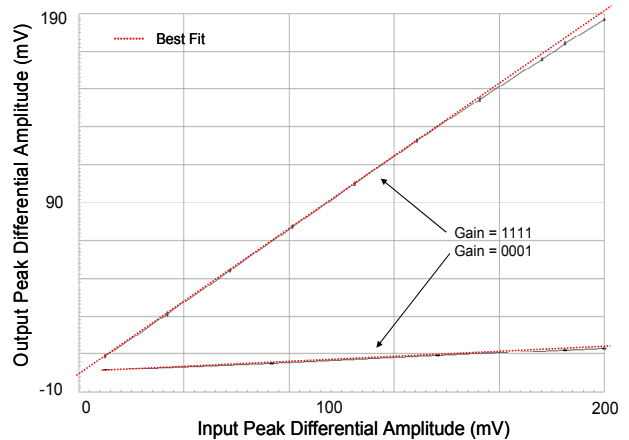


Figure 7. Linearity with Increasing Input Signal

The input signal to the multiplier is AC coupled to enable the differential pair (M1 & M2 in Figure 4) to be properly biased. For this circuit the input capacitor was set to 10 pF to obtain a very low high-pass pole. This was designed as such to facilitate a multiplier that can be used independent of application. For example a transversal filter used for equalization in fiber transmission will require low frequency operation to deal with potentially long strings of ones and zeros. The 10 pF input capacitor allows this low frequency operation. However, not all applications have this requirement. In chip to chip commu-

nications if data encoding, such as 8b/10b encoding, is used the maximum length of a strings of ones and zeros are restricted and such an aggressive high-pass pole is not required. This results in a smaller required size for the AC coupling capacitor which is an important consideration as the 10pF input cap has a significant bottom-plate capacitance. This presents an extra load to the delay circuit and can serve to reduce the bandwidth at the multiplier delay interface.

Figure 8 illustrates the AC response with various gain settings. The low frequency cutoff is around 20 MHz and the high frequency cutoff is around 9 GHz. For a 10 Gbit/s data stream the maximum frequency of the data is $1/(2 \times \text{Bit time})$ which is 5 GHz. Thus a high frequency cutoff above 5 GHz should ensure all data bits are received.

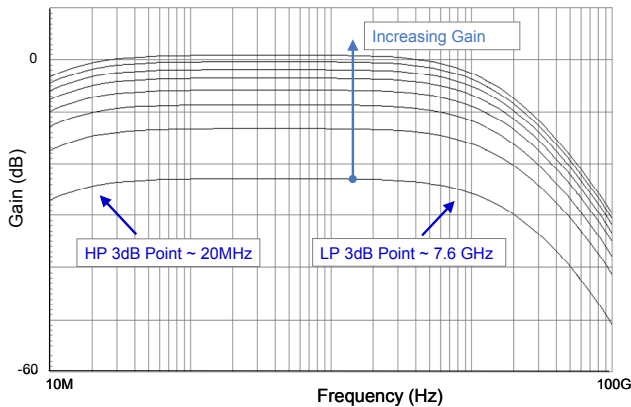


Figure 8. AC response of Multiplier

In the passband the gain is flat. This ensures that all data, regardless of its spectrum, will experience the same gain.

A summary of the pre-layout and post-layout simulations can be seen in Table 1.

Table 1: Summary of Multiplier

Multiplier Parameter	Performance Pre-layout	Performance Post-layout
Supply Voltage	1.2 V	1.2 V
Total Power with Maximum Gain setting	1.7 mW	1.78 mW
Linearity Error	< 2%	< 2.5%
Minimum 3dB Bandwidth	9.3 GHz	7.6 GHz

V. CONCLUSIONS

Equalization is a powerful technique used to remove ISI from data transmitted through a medium. There are

various ways to implement equalizers and this paper focuses on the continuous time FIR filter. Specifically, a multiplier design is introduced as a building block for such a filter.

The multiplier is based on an LNA architecture and is designed for high frequency operation using a low supply voltage. The multiplier utilizes cascode transistors to reduce the Miller effect and by keeping the cascode transistors small the capacitive loading at the summing node is minimized. The loading at the summing node is further minimized through the introduction of the swap switch. This switch allows negative gain without doubling the gain stages and hence the capacitive load at the summing node is reduced. This not only increases the bandwidth of the multiplier, but also allows an increase number of taps leading to improved recovery from ISI.

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