A 2.4GHz Wide Tuning Range VCO with Automatic Level Control Circuitry

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Abstract

This paper presents a VCO with automatic level control circuitry. This feedback mechanism helps to keep the VCO at an optimum level for best phase noise performance over temperature, process and frequency variations. The VCO was fabricated in a 50GHz SiGe BiCMOS process. It uses MOS varactors to achieve a 600MHz tuning range. The phase noise of the VCO was measured to be \(-97\text{dBc/Hz}\) at 100kHz offset from the carrier. This number was constant to within a couple of dB under all conditions. The VCO drew approximately 4mA from a 3.3volt supply.

1. Introduction

Recently there has been much interest in the prospect of voice over IP (VOIP) services for the home. This would be added to cable TV and internet access provided by wall boxes that sit outside the home. To provide VOIP requires that the cable modem wall box be powered over the cable to allow emergency lifeline service in the event of a power failure. This means power consumption and consistent operation meeting DOCSIS (Data-Over-Cable Service Interface Specification) over a wide range of operating temperatures \((-40\degree C \text{ to } +85\degree C)\) will be driving specifications for these wall boxes and any telecommunications chips that will be used in them.

This has led to much interest amongst many companies in doing highly-integrated cable tuner receiver chips. Since these chips must be capable of delivering high quality 256QAM demodulated signals to the baseband processor, phase noise performance of any VCO must be of good quality and is one of the most important design considerations in the receiver. Also since cable is broad band \((47-870MHz)\) these VCOs must be tunable over a broad range \((-1GHz)\). Even with these stringent requirements, SiGe technology is now at a point where it is feasible to generate such VCOs on-chip with the rest of the receiver circuitry. This paper presents a VCO, which is a prototype for meeting such specifications.

2. VCO Design

The purpose of this design was to create a VCO with a wide tuning range, good phase noise and very robust performance over process and temperature variations. The requirement for as much tuning range as possible makes the cross-coupled \(-G_{m}\) oscillator topology the only viable option. The VCO schematic with additional feedback circuitry is shown in Figure 1.

![VCO topology with feedback in the bias to control the amplitude.](image)

The current in the VCO is set by transistor Q5 which acts as a current source. Transistors Q1 and Q2 form the negative resistance across the LC tank formed by \(C_{var}\) and \(L\). Coupling capacitors \(C_{cp}\) are included so that the bases of Q1 and Q2 can be biased at a DC voltage less than the collector’s DC voltage. This allows the voltage swing at the collectors to grow to an acceptable level without saturating the transistors. Simulations have shown that this is a very important design consideration as once these transistors start to enter saturation at the top and bottom of the oscillation swing the phase noise...
performance of the oscillator is greatly reduced. The capacitors $C_{cp}$ are set so that their impedance is large compared to the input impedance of the base of Q1 and Q2, but small enough so that their parasitic capacitance does not have a large effect on the oscillation frequency.

The inductor in the tank was implemented using a differential geometry and biasing for the tank is provided through the centre tap of this structure [1]. Together with the varactors, the inductor sets the frequency of oscillation in the tank. The varactors themselves were implemented using MOS varactors as described in [2][3] since these structures feature a high tuning ratio and high Q. Diode D1 is included to reduce the voltage at the tank one VBE below the supply to allow the varactors to take full advantage of their tuning range. The MOS varactor’s C-V curve is centred around zero volts and the full capacitance range is achieved by applying plus or minus one volt to the device. Slightly greater tuning range could be achieved if the tank voltage was reduced more, however this would start to affect other performance aspects of the design.

Transistors Q3 and Q4 are used to limit the swing of the oscillator to slightly more than one VBE. Once the oscillation gets this large, these transistors start to turn on briefly at the top and bottom of the oscillator’s swing, loading the tank with their dynamic emitter resistance. This will effectively de-Q the circuit and prevent the signal from growing any larger. This will prevent transistors Q1 and Q2 from entering saturation. However, if transistors Q3 and Q4 have to be heavily turned on to limit the swing they will also start to affect the phase noise performance of the circuit.

3. The AGC Feedback Loop

The transistors Q3 and Q4 limit the amplitude of the oscillation directly but are also the basis for the feedback loop that is the second mechanism used to make sure that the VCO is operating at an optimal level. Once these transistors start to turn on they start to draw current $I_f$. Their collectors are connected back to the drain of the PMOS device M1. The gate of M1 is connected to a reference that is generated by a bandgap circuit (omitted for simplicity). Q3 and Q4 then steal current away from M1 causing the current in Q6 to be reduced. This in turn reduces the current in the VCO. Since the VCO amplitude is related to its current this in turn reduces the amplitude of the VCO until the transistors Q3 and Q4 just barely turn on. This ensures that the VCO always draws just enough current to turn on these transistors and no more, even though the reference currents may vary for any number of reasons. The reference current through M1 must therefore be set higher than the optimum as the loop can only work to reduce the current through the oscillator, but can never make it higher.

The loop can be drawn conceptually as shown in Figure 2. The point P shown in Figure 1 acts as a summing node for the three currents $I_{tank}$, $I_{bias}$, and $I_f$. The current mirror amplifies this current and produces the tank current, which is taken by the VCO core and produces an output voltage proportional to the input tank current. The limiting transistors at the top of the tank convert the VCO amplitude and convert it into a current that is fed back to the input of the loop.

The transfer function for the various blocks around the loop can now be derived. In the current mirror two capacitors $C_1$ and $C_2$ have been placed in the circuit to create two dominant poles in the system and limit the frequency response of the loop. Assuming the capacitors’ impedance is much smaller than $r_T$ the transfer function for this part of the loop can be approximated by:

$$A_1(s) = \frac{I_{tank}(s)}{I_{bias}(s)} \cong \frac{g_m \frac{s}{C_1}}{\left( s + g_m C_1 \right) \left( s + g_m C_2 \right)}$$

(1)

The behaviour of the oscillator must also be determined in so far as it effects the behaviour of the loop. Performing an analysis similar to that in [6] it can be shown that the VCO amplitude can be approximated as:

$$V_{tank} = I_{tank} R_T$$

(2)

where $R_T$ is the equivalent parallel resistance of the tank. This formula has obvious limitations in describing certain aspects of oscillator performance. Specifically, for large amplitudes the oscillation amplitude will cease to grow with increasing current and for low current the VCO will not start. This expression also fails to capture the frequency response of the oscillator amplitude.

For the purposes of this analysis the oscillator tank is treated as a resonator with a pulse of current applied to it by transistors Q1 and Q2 each half cycle. This second order transfer function can be written in the time domain as:

$$v_{var}(t) = \frac{2 e^{\frac{-t}{\tau_C}}}{C_{var}} \cos(\omega_o t + \phi_o)$$

(3)

where $\omega_o$ is approximately equal to the frequency of oscillation and $\phi_o$ is an arbitrary phase. From this equation the transient behaviour of the circuit can be determined. The time constant $R_T C_{var}$ in (3) is equivalent...
to a pole in the response of the oscillation amplitude versus bias current. This pole can be added to give frequency dependence to (2).

\[ A_z(s) = \frac{V_{tank}(s)}{I_{tank}(s)} = \frac{1}{C_{var} + \frac{1}{R_f C_{var}}} \quad (4) \]

It is interesting to note that a tank with higher Q will respond slower and therefore have a lower frequency pole than a low Q oscillator. This makes intuitive sense since it is up to the losses in the tank to cause a change in amplitude.

The last part of the loop consists of the limiting transistors. Their transfer function can be written as:

\[ A_i(s) = \frac{I_r(s)}{V_{tank}(s)} = K \quad (5) \]

where \( K \) is a constant. Here it is assumed that this part of the loop has no significant frequency response and the amplitude and current are just related by some constant. In reality this transfer function will be very non-linear.

These equations can be used to design the loop and demonstrate the stability of this circuit. The capacitor \( C_2 \) is placed in the circuit to create a dominant and controllable pole and to clean up noise from the bias. However, since its frequency will be of the same order of magnitude as the pole in the VCO, this creates a potential for oscillation. In order to prevent this, \( C_1 \) introduces another pole and one zero to the system. This splits the two poles in the bias circuit apart creating a dominant pole at a very low frequency, and pushing the original pole to a much higher frequency. The zero and pole roughly cancel at low frequency so minimal phase shift occurs except at higher frequencies where there is less gain.

More phase margin is required, especially if there is uncertainty as to the Q of the VCO. A high Q VCO will lead to a less stable loop as it will have more phase shift at lower frequency.

4. Experimental Results

A prototype VCO was fabricated on a test chip along with many other circuit building blocks. It was packaged in a TQFP forty pin package for evaluation and was mounted on a test board. A photomicrograph of the VCO is shown in Figure 3. It uses a differential octagonal spiral inductor with a patterned ground shield[4]. The inductor was designed with the help of ASITIC[5] and has a measured differential Q of about 10 at 2.4GHz. The chip area used by the VCO core and associated circuitry was approximately 1.2mm X 0.8mm. Bond pads are not included in this dimension because in an actual application they would not be used.

The VCO output was buffered through a circuit designed to reduce any loading on the tank by associated circuitry. Measurements reported here are on the performance of the stand alone VCO, however it has also been demonstrated in a synthesizer. The circuit ran off a 3.3V supply, drew 4mA of current and produced a nominal output power of about –8dBm. The output power of the VCO varied slightly across the operating band, however this was due to the frequency response of certain elements in the signal path on the board. The tuning characteristic of the VCO with input voltage is shown in Figure 4. Note that most of the tuning range is achieved between 2V and 3.3V. This is due to the tuning characteristic of the varactors in this process. In some processes the varactor tuning curves can be centered around a voltage other than zero volts which would be beneficial as it would center the tuning curve closer to the mid point between ground and VCC. However, these varactors do produce a very nice linear curve, which is good for the synthesizer design. The \( K_{VCO} \) as measured from this graph is about 400MHz/Volt.

![Figure 4. Plot of the VCO frequency vs. tuning voltage.](image)

The phase noise of the circuit was measured with a phase noise measurement system using a discriminator method as well as with a spectrum analyzer. Both methods gave consistent results. Five samples on
different boards were measured at different points in the tuning range. The phase noise was found to vary by less than one dB regardless of board or carrier frequency. A typical plot taken from one of the boards set to a carrier frequency of 2.2GHz is shown in Figure 5. This shows the typical performance of this VCO of –97dBc/Hz at 100kHz offset.

![Figure 5. Plot of the VCO phase noise vs. frequency offset from a 2.2GHz carrier.](image)

The phase noise and output power were also measured over a -40°C to 100°C temperature range. The phase noise was found to be almost constant over this range, changing by only a couple of dB. The power also changed slightly over this same range. This is most likely due to changes in the V_BE needed to turn on the limiting transistors. The results of this measurement are shown in Figure 6.

![Figure 6. Plot of the VCO power and phase noise at 100kHz offset vs. temperature.](image)

Figure 7 shows a comparison of measured phase noise over the tuning range compared to simulated phase noise with and without the feedback circuitry. The circuit without feedback had the current carefully set in simulation for best results, while other simulation was done on a circuit that matched the measured one. Simulation was a couple of dB optimistic, but it is clear how the feedback works to keep the phase noise constant. This is due to an AM to FM conversion process that is reduced by the presence of the limiters and feedback circuitry. If they are removed the effect is dramatic in the areas where the oscillator has high gain.

![Figure 7. Plot of simulated and measured phase noise versus carrier frequency.](image)

5. Conclusions

This paper has presented a VCO with a phase noise of –97dBc/Hz at 100kHz offset. The VCO had a very wide 27% tuning range. The output power and phase noise was almost constant over a temperature range of –40°C to 100°C. The design of the feedback automatic gain control circuitry that helps to achieve this performance has been discussed including loop stability issues.

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7. References