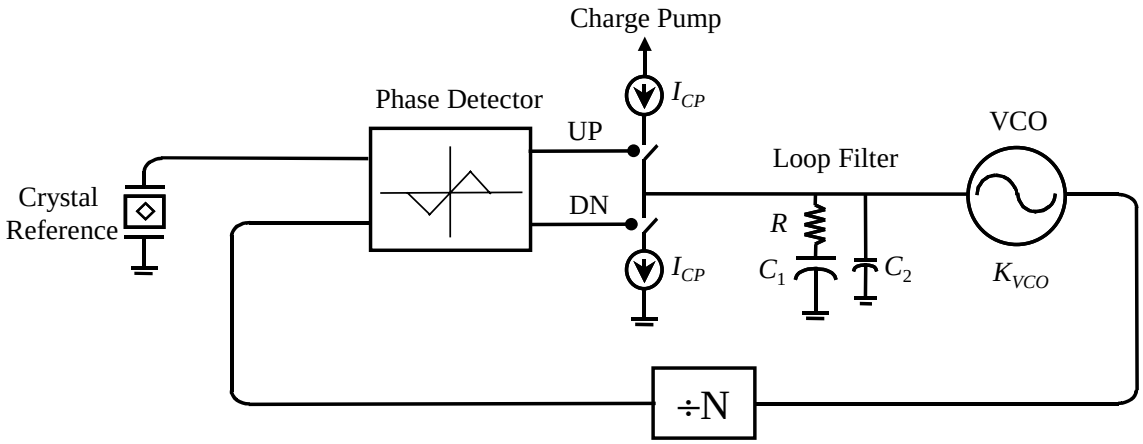
ELEC 5705 Synthesizer Integrated Circuit Design:
Assignment #1

Due Feb. 15th, 2005 (BEFORE CLASS)

The goal of this course will be to design using Cadence Design Systems a completely integrated frequency synthesizer. This first assignment will be to design the system architecture and to explore the system level performance. A rough guide for the synthesizer specs will be as follows:

- Center Frequency of the VCO: 5GHz
- Tuning Range: 4.8GHz – 5.2GHz
- K_{VCO}: 135MHz/V
- Divide Ratio 125
- XTAL frequency: 40MHz

For the first assignment you should build a loop as follows:



You should build all components out of behavioral blocks. No transistors! Also note that the VCO and divider can be combined to save simulation time for most of the assignment.

For the tri state phase detector circuit:

1) Set the loop bandwidth to 150kHz and show settling for a 20, 60, and 200MHz step in frequency for ζ = 0.5, 0.707, and 1.3 (try this part with the XOR as well for a 200MHz step at ζ = 0.707).
2) For ζ = 0.707 adjust the loop bandwidth to 20kHz, 200kHz and 2MHz and compare settling for a 100MHz step in all cases. What is the maximum BW that the loop remains stable?
3) Assuming that the VCO has a phase noise of –100dBc/Hz at 100kHz offset (20dB/dec slope), the CP puts out an average noise voltage of 10pA/√Hz and the crystal has a phase noise floor of –150dBc/Hz ($Q_L = 8*10^4$), estimate the phase noise for the settings in part 2. What is the integrated jitter from 100Hz to 10MHz offset?
4) Design an AHDL based programmable divider. Run one or two simulations to verify that it works in the loop. Note you will need this later! It should have approximately 5 control bits and should have a step size of one.