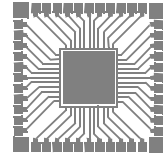




**Carleton**  
University

# The Microelectronics Bridge Camp 2000



Strategic  
Microelectronics  
Consortium

Carleton, May 29 to June 9

McGill, May 15 to May 26

## Program Highlights

### Convert New Grads Into ASIC Designers.

The program is designed to take fresh Electrical Engineering graduates and give them intensive training in ASIC design. However persons with related background, like technical marketing, computer engineering, and board design have all very successfully completed the Camp.

### Two 2-Week Courses:

- One For Digital ASIC Design,**
- One For Analog ASIC Design.**

The analog and digital courses at Carleton run concurrently the first two weeks in June. The McGill courses both run concurrently the last two weeks of May. Students may take both the analog and digital courses by switching from Montreal to Ottawa.

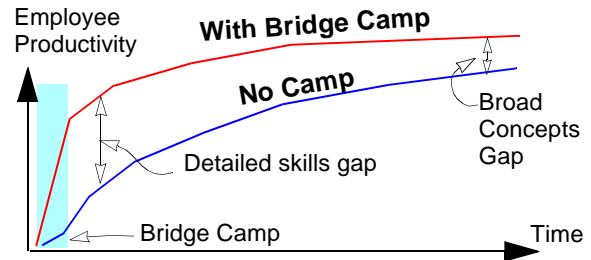
### Joint Industry-University Participation In Content And Delivery.

The course was originally designed by the Strategic Microelectronics Consortium (SMC) after consulting a large number of managers in their member companies. Also industrial seminars are given every day on topics such as intellectual property and design reuse. Industry has been very generous in supplying exceptional speakers as you will see if you check the lists inside.

### A Team Design-Project Is An Integral Part Of The Course.

Teams of four do an ASIC design project. The project at Carleton is a spread-spectrum transceiver. The McGill project is a PCI and USB computer interface.

### Fast Ramp-Up



Initially the intensive camp training should bring a new employee up to speed much faster than osmosis training on the job. In the longer run the camp exposure to broader concepts like testing, market windows, and design reuse should help maintain the productivity gap.

### Industrial CAD Tools Used

The major tools used in the course are the Canadian Microelectronics Corp suite of tools. For example the Carleton Digital Camp will use Synopsys tools for synthesis, timing verification, scan insertion and test vector generation. Verilog XL for pre and post layout simulation, and Cadence Silicon Ensemble tools for floor planning, and place and route. The process libraries will be for TSMC's 0.35 $\mu$ m, double poly, triple metal process.

### Industrial Tours

The camps have always had a tour of a fabrication plant, a test facility, a reverse engineering facility and a reworking/repair lab. Many new graduates find these experiences eye opening. For example, most are not aware that a error in a prototype IC may be economically repaired to allow further testing.

## About SMC

The Strategic Microelectronics Consortium (SMC) is the industry's not-for-profit national association dedicated to accelerating the development of microelectronics in Canada. The members of SMC collectively account for over 90% of the microelectronics activity and business revenue in Canada. SMC's program focuses on projects to increase the supply of skilled microelectronics workers and ease their transition into industry; to attract advanced silicon capability to Canada and to build a national and international awareness of Canada's microelectronics capabilities.

## About The Bridge Camp

First run at Carleton in 1997, the Bridge Camp has trained over 125 recent engineering graduates on the subtleties of ASIC design. Based on the success of the first camp, and Canada's strong need, SMC expanded the program to three Universities in 1998. Carleton and McGill continued the Camp in 1999 and in 2000. The program is noted for the strength of its instructors -a mixture of designers from industry and from academia-, its curriculum -which went through extensive revisions with industry-, and its use of industrial design tools. It is also infamous for the amount of homework required.

## A Summary of the Two Carleton Courses.

1. The mostly **digital course** takes students from a customer's "fuzzy specifications" through high-level simulation (Simulink) to a circuit design for standard-cell ASIC. The design at Carleton will be done using Verilog. Emphasis will be on writing synchronous, synthesizable code starting from the initial simulation phase. Possible problems with clocking, testing, off-chip inputs will be treated. The chip will be taken through to final tape-out using Synopsys and Cadence tools. The course is given by the faculty at the University who are involved in VLSI design, but are supplemented by many industrial speakers who stress concepts such as customer-owned tooling, intellectual property, packaging, testability and various cost-time trade-offs.

2. The **analog**-layout-fab course gives an

introduction to analog circuits: op-amps, switched-capacitor, analog-to-digital conversion, RFIC, process basics and memory internals. Another major emphasis is the analog side of digital; gate speed and loading, failure modes (e.g. hot-carriers, electromigration, and latchup), transmission-line effects, package models and ESD. They will design and layout the analog parts of the project, and merge them with the previously designed digital parts. At this stage, floor planning, layout, extraction, testing, packaging, and interfacing with a foundry will be considered.

## The Course Project

The project is a central part of the course and provides reinforcement for the lectures. It is a mixed analog-digital circuit. The digital part (1000-3000 gates) can be completed in two weeks albeit with considerable coaching.

We force attention to milestones; the groups present their own management plans, which have to pass review. If they are behind schedule, they have to "buy" a piece of design from a competing group or "off the shelf" from the Camp. The groups treat the designs as noncompetitive. All students attend the design reviews of other groups and are encouraged to talk over problems with other groups. Also camp staff are available to give help and advice for more than a reasonable time each day.

This year's project will be a spread-spectrum receiver-transmitter. This project has been used since 1998 at Carleton and turned out to be a close match to the students abilities plus it is of topical interest to students in communications. The digital course students design the spreading and QPSK modulators. They also design the correlator for the receiver, the hardest part of the digital project.

The analog students add an analog input with an oversampled A-to-D, which uses an op-amp and comparator. The students design components of a folded-cascode opamp, to give the required performance. Pads and a final output integrator are also added to the circuit. Possible RF portions will be discussed but will not be part of the project.

# The Digital ASIC Design Course



- **CMOS Process Overview**  
CMOS process; Steps in deep submicron fabrication. Silicon Run video with many "real time" comments. Where digital circuits are going; SIA Road map. (Joint with Analog Camp).
- **CMOS Review**
- Gate properties; delay, loading, fan out, fan in, power, gate construction. Gate properties in Verilog.
- **Standard blocks, Function and Structural**  
Verilog Examples: Mux, demux/priority encoders, shifters, barrel-shifters. Verilog models.
- **Standard Blocks and Procedural Verilog**  
Counters: binary, Gray-code counters, pseudorandom (LFSR) and applications. Procedural Verilog models.
- **Synchronous machines, Verilog for Synthesis**  
FSM, state encoding, one-hot, synchronous test benches.
- **Testing Overview**  
Faults and defects, fault modelling, ATPG, sequential test, scan, BIST, SCANBIST, boundary scan.
- **Verilog HDL as a language**  
Synthesis vs simulation: Gotcha's, asynchronous circuits, alternate clock example, ripple-counter code, test-bench code, coding style, examples.
- **Synchronous clocking**  
Skew, optimization for timing, false paths, harmonically-related clocks, resynchronization, skew-correction latching, clock gating, arbiters.
- **Avoiding "work mostly" circuits**  
Asynchronous inputs, safe state-assignment, synchronizing flip-flops, safe reset circuits. Avoiding multiple-bit input problems; handshaking, debouncing, Gray codes. Leads into metastability.
- **Metastability.**  
Exponential model, MTBF, maximizing MTBF, safe state assignments, arbiters. Short lecture.
- **Clock distribution:**  
Clock trees, central clock distribution, line-widths, buffering principles. Power considerations. Grover loop.
- **Design Flow**  
Flow for a submicron process. Simulation and problems, timing verification, timing files, meeting delay constraints, floor planning.
- **ASIC Implementations: FPGAs:**  
Standard-cells, gate arrays. FPGAs, design cycles compared. FPGA architecture: Technology (fuses, antifuses, SRAM, charged gates). Components (logic elements, IO blocks). Performance (routing, logic vs ff).
- **Phase-Locked Loops and Applications.**  
Components: phase detectors and charge pumps, oscillators, dividers. Applications: clock-recovery, carrier recovery, frequency synthesis.(Joint with Analog Camp)
- **Digital Signal Processing.**  
Significance of the math: aliasing, accurate interpolation, possible nonlinear interaction. Complex resonators: poles-zeros and structure of simple filters. Biquads, cascaded filters, the reverb/comb filter, linear-phase/all zero/FIR filters. Adaptive filters, the LMS algorithm. Quantization, modelled as noise, problems with model, limit cycles, scaling, noise shaping.
- **Memories**  
Block-level internals; commodity SRAM, DRAM, SDRAM interfaces; memory in a logic process, memory in FPGAs. (Joint with Analog Camp)
- **More Information**  
[www.doe.carleton.ca/Bridge\\_Camp2000](http://www.doe.carleton.ca/Bridge_Camp2000)

# The Analog ASIC Design Course



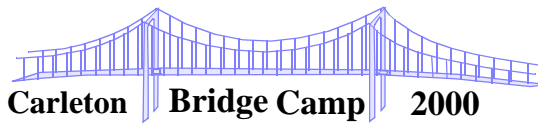
- **Overview of Analog.**  
Why analog? Design and layout features of MOS: transistors, capacitors, resistors and diodes. Analog blocks: voltage references, general properties of differential circuits.
- **Operational Amplifiers, Design, Simulation and Layout.**  
Building Blocks: current sources, gain stages. Types: two-stage, telescopic, folded-cascode. Design Considerations: noise, gain, slew rate bandwidth, stability, common-mode considerations.
- **Switched-Capacitor Circuits:**  
Basic concepts, differential circuits. Multi-phase clock generators. Pedestal effects, Clock feed-through, Noise (KTC noise).
- **Data Conversion.**  
Digital-to-Analog: R-2R ladder, current-steering, linearity. Analog-to-Digital: Successive approximation, flash converters, two-stage flash.
- **Oversampled A-to-D:**  
Concepts, noise shaping, 1st order, higher-order, multi-stage noise shaping (MASH).
- **Overview of RFICs and Broadband Challenges and Techniques.**  
Low-noise amplifiers, mixers, oscillators, power amps, synthesizers, on-chip inductors, packaging. High-frequency simulation and modelling.
- **Memory Testing**  
Memory testers fault models, conventional tests. RAM in logic, RAMBIST.
- **Dynamic logic**  
Gate types, latch types, interface problems. Uses for fast high-density logic. Less aggressive uses: resynchronizing latches, reduced power TSPC flip-flops.(Joint with Digital Camp)
- **Layout Considerations and Reliability:**  
Standard cells, pads, protection, buffers, EMI, grounds, power, latchup, electromigration. (Joint with Digital Camp)
- **Submicron CMOS Process Steps.**  
Reasons behind design rules, scaling, component matching. Choosing technology, bipolar/CMOS/biCMOS/SiGe. Analog design in a digital process. (Joint with Digital camp)
- **Real Submicron MOSFETS**  
MOS review, short-channel effects, hot carriers, sub threshold operation, velocity saturation. Advanced SPICE models.(Device 2)
- **Layout 1**  
Lab talk: Floorplanning, design rules, extraction, verification, LVS.
- **Layout 2**  
Lab talk: Good layout, VDD & VSS, electromigration, placement, capacitors, crosstalk, grounds.
- **More Information**  
[www.doe.carleton.ca/Bridge\\_Camp2000](http://www.doe.carleton.ca/Bridge_Camp2000)

# Carleton Camp: Industrial Lectures and Site Visits

These were the lectures/tours arranged in 1999. The Carleton analog course was cancelled because of low attendance. The 2000 speakers are presently being arranged.

- **Designing Products that Win.**  
Moore's technology adoption life cycle, time-to-market, immature-mature products, technology-design-customer interaction.  
(Jim Roach, Tundra)
- **The Semiconductor Design Business**  
Technology market drivers, good and bad examples of products, leading edge vs bleeding edge.(Dennis Colburn, DC Technologies)
- **Team Project Management**  
People-oriented and task-oriented persons, four-quadrants of personal style.  
(Tony Stansby, SMC)
- **Digital IC Testing in a Business Environment**  
IC product development cycle, tester hardware and signals, typical tests, test fixtures, characterization, impact on business.  
(K. Fai Chen, Mitel)
- **Shrinking Technology**  
Effects on design, CAD, and designers.  
(Stan Mazor, Cadabra)
- **Site Visit**  
Production fabrication and testing lab.  
(Nortel Networks)
- **Design Analysis and Intellectual Property.**  
Protection of IP, patent uses and limitations, reverse engineering, student analysis from photos. (L. Lam, Semiconductor Insights)
- **Design Reuse**  
Design reuse, virtual components, business and legal issues, design-for-reuse/design-with-reuse. (Parvis Yousefpour, Nortel Networks)
- **Design for Testability and Reliability**  
Testability, reliability, pure synchronous design, scan, BIST, JTAG and board testing,  
(Karl Siemens, Telexis)
- **Reworking/ Testing, Microsurgery.**  
Methods of repairing prototypes and capabilities of a reworking laboratory.  
(M. Simard Normandin, Nortel Networks)
- **Issues in Analog Design**  
Design flow including humans, models, tool interaction, common gotcha's -amplifier loading, power leads, parasites, digital models aren't, suspect transistor models, matching is not well known, simulate power up and down...-, document your design concepts  
( Ed MacRobbie, Philips)
- **Practical Mixed-Signal Test**  
Comparing costs -pins vs area, yield vs fault coverage, area vs time-to-market, area vs test time-; analog test methods -P1149.4 mixed bus, mixed BIST 3 examples.  
(Steve Sunter, Logic Vision)
- **Phase-Locked Loops**  
Uses, basics, VCOs, loop dynamics, phase-frequency detectors, charge pumps, delay-locked loops. (Stanly Ma, Mosaid)
- **Reverse Engineering Lab**  
Tour of Semiconductor Insights analysis laboratories.
- **Rework/Cost-Reduction**  
For high volume, fast ramp-up, long life products. Improving process, die size, package, test-time, yield.  
( Ray Wong, Nortel Networks)
- **Packaging**  
SMT families, parasites and noise, thermal, moisture, esd, handling and soldering, MCMs telecom packaging. (Reg Simpson, Nortel Networks)
- **Memory**  
Static and dynamic ram, principles and innovations especially embedded memories.  
(Peter Gillingham, Mosaid)
- **Analog design traps**  
Substrate emissions, thermal problems, power supply noise, package problems.  
(Tony Brown, Nortel Networks)
- **More Information**  
[www.doe.carleton.ca/Bridge\\_Camp2000](http://www.doe.carleton.ca/Bridge_Camp2000)

# The Academic Faculty



## Carleton- A Hotbed for VLSI and Communications

Carleton Electrical Engineering, largely because of its proximity to large hi-tech companies, has specialized in VLSI, telecommunications and computers. Its faculty are noted for innovations such as the switched-capacitor filter, and the Boothroyd transistor models. Almost all the faculty are involved in joint research with hi-tech companies, and graduate students in VLSI often have an industrial mentor for their program.

## The Academic Instructors

**Prof. Calvin Plett** will be teaching analog design. Engineers from the Ottawa area may be aware of his very popular graduate course on RF IC-design. His teaching style and the way he relates it to his extensive practical experience tend to overfill his courses. His research and teaching cover switched-capacitor and analog filters, phase-locked loops, A/D converters and of RF circuits. He also "coaches" the "stress relief volleyball" between bridge-camp lectures.

<http://www.doe.carleton.ca/~cp>

**Prof. Garry Tarr** teaches the semiconductor and IC fabrication concepts. He has worked with SOI CMOS, and Si-Ge as well as CMOS and bipolar technologies. Garry is in charge of the Carleton fabrication lab which has CMOS capability and can use electron-beam write to achieve a 0.2 $\mu$ m feature size. For more about the laboratory check the fab's web page.

[http://www.doe.carleton.ca/fab/fab\\_lab.html](http://www.doe.carleton.ca/fab/fab_lab.html)

Check Garry's web page for a lot about canoeing in Algonquin Park.

<http://www.doe.carleton.ca/~ngt/algonquin/intro.html>

**John Knight** is the professor who will be teaching much of the digital-circuit design, testing and layout. John has taught digital

design and testing courses at Carleton and at Nortel and has won several teaching awards. His research interests centre on low-power circuitry and behavioural synthesis. His students also know him for metaphors like "blaspheming the clock."

<http://www.doe.carleton.ca/~jknight>

**Prof. Ralph Mason** expertise spans digital ASICs, analog ASICs, FPGAs, DSP, and communications protocols. At Carleton he has supervised many graduate students most of whom have submitted ASIC designs and has done extensive consulting on mixed-signal ASICs at Philips.

<http://www.doe.carleton.ca/~rmason>

If you can't find **Prof Tom Smy** in his office, check the squash court. Tom is a metalization specialist who applies his knowledge to interconnects, on-chip inductors and CAD. Last year he gave the Camp an overview of deep submicron interconnect especially how it affects design.

<http://www.doe.carleton.ca/faculty/smy/>

**Trevor Rainey** of St. Lawrence College will manage the camp again this year. Trevor keeps the lecturers on topic, watches for battle fatigue, coordinates with industry about students and speakers, and sprays WD40 on the rough spots. In his other job, he coordinates a very successful industry-college joint project program.

- **More Information**

[www.doe.carleton.ca/Bridge\\_Camp2000](http://www.doe.carleton.ca/Bridge_Camp2000)

# The Microelectronics Bridge Camp

May 29 to June 9, 2000

## The Carleton and McGill Courses

- Year 2000 courses will be held at both Carleton and McGill Universities. The courses will be quite similar, with the major differences tabulated below.
- The analog and digital courses will run concurrently in both Camps. Students wishing to take both analog and digital courses should register for one at McGill and the other at Carleton.

### Technical Differences, Carleton and McGill

	Carleton University	McGill University, see <a href="http://www.mcgill.ca/conted/">www.mcgill.ca/conted/</a>
Analog Course	May 29 to June 9 Mon-Fri	May 15 to 26 Mon-Fri
Digital Course	May 29 to June 9 Mon-Fri	May 15 to 26 Mon-Fri
Design Language Used (Digital Course)	Verilog	VHDL
Project Emphasis	Spread Spectrum Transceiver	Computer interfacing using PCI and USB buses
Location	Carleton University, Ottawa	McGill University, Montreal
More Info	<a href="http://www.doe.carleton.ca/Bridge_Camp2000">www.doe.carleton.ca/Bridge_Camp2000</a>	<a href="http://www.mcgill.ca/conted/">www.mcgill.ca/conted/</a>

## The Carleton Camp

### Registration Fees and Deadlines for the Carleton Bridge Camp

Completed registration form, with payment or purchase order received on or before Friday, April 14-

**\$ 4,100** per person for non-SMC members, **\$3,900** per person for SMC Member Companies.

Completed registration form, with payment or purchase order received after April 14, but on or before Monday, May 1-

**\$4,300** per person for non-SMC members, **\$4100** per person for SMC members.

### Cancellation Policy, Carleton Bridge Camp

Written cancellations will be accepted if received on or before Monday, May 1. However a \$50 cancellation fee will be assessed. After May 1, full fees will be invoiced. Substitution is permitted at any time at no extra charge.

If there is insufficient attendance to conduct either Carleton course, notice will be given registrants on Friday, May 5

# The Microelectronics Bridge Camp at Carleton

## Registration Form

Registrant Information:	
Please register me for: the CMOS <b>Analog</b> ASIC Design _____ or the CMOS <b>Digital</b> ASIC Design _____ Both courses run concurrently, May 29 to June 9, 2000.	
Name	Position
Organization:	E-mail:
Address:	Telephone (    )
Address:	Fax: (    )
Address:	Background, for example: new EE grad, board designer, C programmer etc;
Province, Postal Code	
Registrant's Signature:	Date
Billing Information (See previous page for fees)	
Contact person:	Include address where it different from above
Telephone: (    )	Organization:
e-mail:	Address
Fax: (    )	Address
	Province, Postal Code

Please return this registration form to:

Janet Tite,  
Strategic Microelectronics Consortium  
50 Hines Road, Suite 240  
Kanata, ON K2K 2M5  
CANADA  
Fax: (613) 271-1896  
e-mail janet@smc.ca

Make checks payable to:

*The Strategic Microelectronics Consortium*

Registrants who do not attend the course or cancel after May 1, 2000 are responsible for the full registration fee. Substitutions may be made at any time with no charge.

Registrants who cancel on or before May 1, will be assessed a \$50 cancellation fee.

In the case of changes, Carleton will use e-mail to attempt to contact all registrants, and potential registrants who have contacted SMC/Carleton. However Carleton University reserves the right to make changes, without prior notice, to the course information in printed material, or on the Carleton, McGill, or SMC web pages. This includes alteration to fees or schedules, and revision or cancellation of particular courses. Cancellation fees will be waived for reasons caused by changes in fees, dates, or course cancellation.

If there is insufficient attendance to conduct either Carleton course, notice will be sent to registrants on **Friday, May 5**