quicksynth_timing.txt

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+-------------------------------------------------+
| Report           | report_timing                |
|------------------+------------------------------|
| Options          | > rpt/quicksynth_timing.txt  |
+------------------+------------------------------+
| Date             | 20041204.123918              |
| Tool             | pks_shell                    |
| Release          | v5.13-s022                   |
| Version          | Dec 15 2003 14:22:53         |
+------------------+------------------------------+
| Module           | signed_mult                  |
| Timing           | LATE                         |
| Slew Propagation | WORST                        |
| PVT Mode         | max                          |
| Tree Type        | worst_case                   |
| Process          | 1.00                         |
| Voltage          | 1.62                         |
| Temperature      | 125.00                       |
| time unit        | 1.00 ns                      |
| capacitance unit | 1.00 pF                      |
| resistance unit  | 1.00 kOhm                    |
+-------------------------------------------------+
Path 1: MET Setup Check with pin Z_reg_23/CK
Endpoint:   Z_reg_23/D    (v) checked with  leading edge of 'myclk'
Beginpoint: Breg_reg_1/Q  (^) triggered by  leading edge of 'myclk'
Other End Arrival Time          0.00
- Setup                         0.44
+ Phase Shift                  10.00
= Required Time                 9.56
- Arrival Time                  8.62
= Slack Time                    0.94
    Clock Rise Edge                0.00
    = Beginpoint Arrival Time      0.00
    +-------------------------------------------------------------------------+
    |  Instance  |     Arc       |    Cell     | Delay | Arrival | Required |
    |            |               |             |       |  Time   |   Time   |
    |------------+---------------+-------------+-------+---------+----------|
    |            | clk ^         |             |       |    0.00 |     0.94 |
    | Breg_reg_1 | CK ^ -> Q ^   | DFERPQ1     |  0.42 |    0.42 |     1.37 |
    | i_1        | Bext[1] ^     | AWDP_MULT_0 |       |    0.42 |     1.37 |
    | i_1/i_837  | A ^ -> Z v    | INVD2       |  0.09 |    0.52 |     1.46 |
    | i_1/i_838  | A1 v -> Z ^   | MUXB2D0     |  0.94 |    1.45 |     2.40 |
    | i_1/i_847  | SL ^ -> Z ^   | MUXB2D0     |  0.51 |    1.97 |     2.91 |
    | i_1/i_848  | SL ^ -> Z ^   | MUXB2D0     |  0.61 |    2.58 |     3.52 |
    | i_1/i_426  | B ^ -> S v    | ADFULD1     |  0.60 |    3.18 |     4.12 |
    | i_1/i_737  | B v -> CO v   | ADFULD1     |  0.33 |    3.50 |     4.45 |
    | i_1/i_738  | CI v -> CO v  | ADFULD1     |  0.26 |    3.76 |     4.71 |
    | i_1/i_739  | CI v -> CO v  | ADFULD1     |  0.26 |    4.03 |     4.97 |
    | i_1/i_740  | CI v -> CO v  | ADFULD1     |  0.26 |    4.28 |     5.23 |
    | i_1/i_741  | CI v -> CO v  | ADFULD1     |  0.26 |    4.55 |     5.49 |
    | i_1/i_742  | CI v -> CO v  | ADFULD1     |  0.27 |    4.81 |     5.76 |
    | i_1/i_743  | CI v -> CO v  | ADFULD1     |  0.27 |    5.08 |     6.02 |
    | i_1/i_744  | CI v -> CO v  | ADFULD1     |  0.26 |    5.34 |     6.28 |
    | i_1/i_745  | CI v -> CO v  | ADFULD1     |  0.26 |    5.60 |     6.54 |
    | i_1/i_746  | CI v -> CO v  | ADFULD1     |  0.26 |    5.86 |     6.80 |
    | i_1/i_747  | CI v -> CO v  | ADFULD1     |  0.26 |    6.12 |     7.07 |
    | i_1/i_748  | CI v -> CO v  | ADFULD1     |  0.26 |    6.38 |     7.33 |
    | i_1/i_749  | CI v -> CO v  | ADFULD1     |  0.26 |    6.65 |     7.59 |
    | i_1/i_750  | CI v -> CO v  | ADFULD1     |  0.26 |    6.91 |     7.85 |
    | i_1/i_751  | CI v -> CO v  | ADFULD1     |  0.26 |    7.17 |     8.12 |
    | i_1/i_752  | CI v -> CO v  | ADFULD1     |  0.26 |    7.43 |     8.37 |
    | i_1/i_753  | CI v -> CO v  | ADFULD1     |  0.26 |    7.69 |     8.63 |
    | i_1/i_754  | CI v -> CO v  | ADFULD1     |  0.26 |    7.95 |     8.89 |
    | i_1/i_755  | CI v -> CO v  | ADFULD1     |  0.26 |    8.21 |     9.16 |
    | i_1/i_756  | CI v -> S v   | ADFULD1     |  0.40 |    8.62 |     9.56 |
    | i_1        | Z_long[23] v  | AWDP_MULT_0 |       |    8.62 |     9.56 |
    | Z_reg_23   | D v           | DFERPQ1     |  0.00 |    8.62 |     9.56 |
    +-------------------------------------------------------------------------+
```

Searching for LATE signals (Setup Time Violations)

Use pessimistic models to account for how rise/fall times effect delay

Assume worst case clock skew (if clock tree was inserted)

Use WORST Case Parameters: Low Voltage (1.62V), High Temperature (125C)

Timing Unit is nS

(v) indicates FALLING

(^) indicates RISING

MET or VIOLATED Timing, Setup or Hold Check, Pin that defines endpoint timing

The D input (falling) of flip-flop Z_reg_23 is the endpoint

The Data (rising) from the Q output of Breg_reg_1 is where the path starts

when 'myclk' arrives at endpoint

but the data must be ready a setup time (440ps) before the clock edge

This is the clock-period. The data in this case has one cycle to get from beginning to end

**Clock Period − Setup Time + skew (0) = Required Time**

When the Data actually gets there (See details below)

The timing margin (+ve slack is good)

This column works from the Required time backwards

Clock rises at t=0

Delay from clk rising to Q rising (tcq) = 0.42nS

The net goes into the AWDP_MULT_0 module

The Inverter adds 0.09nS, so TOTAL delay so far is 0.52nS

Note that the critical path is a carry chain through a set of full adders. This is typical in DSP applications.

Data is Required at 9.56nS (T−t_setup)