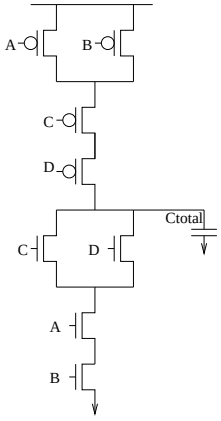
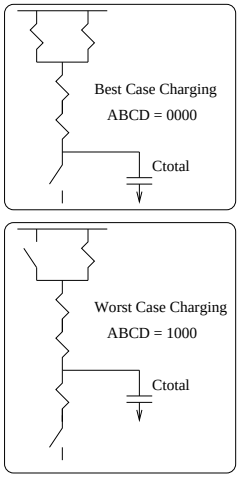
Modelling Complex CMOS gates

Replace each transistor with its equivalent resistance and simplify the resistor network down to one Reff resistance.



WARNING

Reff is 'pattern dependent'



* Assumes all transistors are the same size.

As with the capacitances, it is usefull to define a baseline Rnmin and Rpmin
Rpmin : Resistance of a minimum W/L PMOS in a technology
Rnmin : Resistance of a minimum W/L NMOS in a technology

Beware: These are MAXIMUM channel resistances.
Increasing the width beyond the minimum will lower resistance.

Example: For a given inverter, you know the total load Ctotal=4fF.

Detailed SPICE simulations reveal that tphl = 60ps and tplh = 118ps.
The W/L ratio of the NMOS is 220nm/180nm and is minimum size.
The W/L ratio of the PMOS is 360nm/180nm

Determine the Reff of the PMOS and NMOS. Also determine Rpmin and Rnmin

tplh = 0.69 Rpmos Ctotal

Rpmos = 118ps / 0.69*4f
= 42.75k Ohm

Minimum width is 220nm

360/220 = Rpmin/42.75k
Rpmin = 69.95k

tphl = 0.69 Rnmos Ctotal

Rnmos = 60ps / 0.69*4fF
= 21.74k Ohm

Since this is already minimum sized,

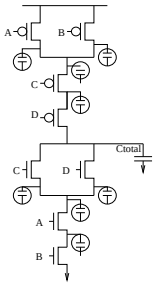
Rnmin = 21.74kOhm

Things we are not taking into account

1) In complex gates there are all of the intermediate drain capacitances which may need to be charged and discharged.

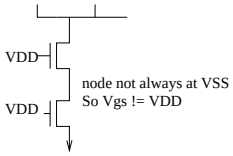
We do account for the Cd capacitances directly on the output node by including them in Ctotal

The others are hard to account for in most cases.
See Elmore's delay model for a good approximation.



2) The approzimation that D = 0.69 ReffCtotal assumes a step input.
For slightly sloped inputs (tr or tf < 1/2 D) it is still a good approximation.

3) In gates other than an inverter, we don't have full Vgs = VDD or −VDD



4) For the same reason as above, since the bulk to source voltage != 0, the effective threshold voltage (Vth) changes

5) We use first order model approximations to get Reff. This does not account for the non−linearities.

Conclusion

Given an arbitrty CMOS circuit with arbitrary transistor sizes,
you should be able to determine the simplified RC delay in terms of Cgmin, Cdmin, Rpmin, Rnmin

Given either technology constants or simulation results, you should bee able to determine Cgmin, Cdmin, Rpmin and Rnmin.