Estimating Effective Resistances in CMOS circuits

Let's simplify a transistor by converting it into an effective resistance (Reff)

Try to coax it into an expression that looks like V=IR or I = V/R and isolate terms to find R

But in charging or discharging a transistor, we go from cutoff −> saturation −> linear −> cutoff

Cutoff Ids = 0

Linear $Ids = W/L * (u e_{ox} / t_{ox})[(Vgs - Vt)Vds - 0.5 Vds^2]$ Often insignificant

$Ids = W/L * K Vds$ Where $K = (VDD-Vt)\, u\, e_{ox} / t_{ox}$

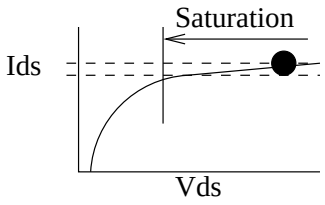
$Ids = 1/R\ (Vds)$

Electron or Hole Mobility

$R = 1/K\ *\ L/W$ depending on whether charging or discharging

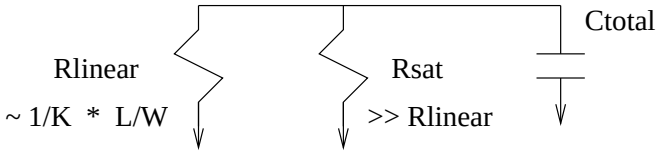
Saturation $Ids = W/L * (u e_{ox} / t_{ox})\ 0.5*[(Vgs - Vt)^2 (1-lambda*Vds)]$

Note that an R does not make as much sense in saturation.
In Saturation, there is a relatively high I, but it is independent of V.



Since Rsat = dV/dI it has a very HIGH instantaneous resistance.

Rsat >> Rlinear



When discharging, the PMOS path is in cutoff, when charging the NMOS path is cutoff.