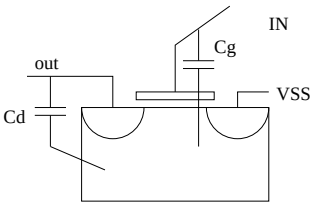
Estimating Average Capacitances in CMOS circuits



For a particular transistor there are 2 capacitances of interest, the gate (Cg) and drain (Cd).

Cg can be estimated as:

$Cg = W * L\ Cox$ where Cox = the capacitance per unit area

Cd is dependent on the layout of the drain but is also proportional to the width.

$Cd \sim= W * Cj$ where Cj = the juniction capacitance per unit width of the drain

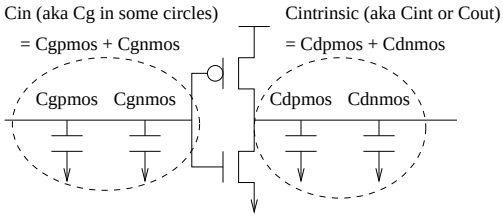
Note: This is simplified from what you might see elsewhere.

In many situations it is usefull to define some base values of Capacitances (and Resistances) relative to the smallest transistor available.

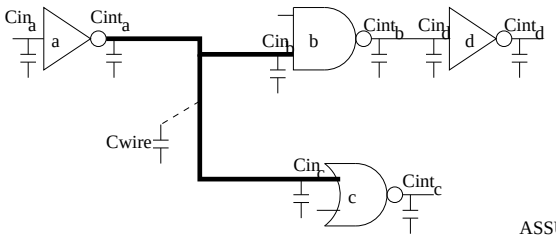
Cg_{min} : The gate capacitance of a minimum sized transistor in a technology (eg. W=220um, L=180um in 0.18um TSMC) .

Cd_{min} : The drain capacitance of a minimum sized transistor in a technology (eg. W=220um in 0.18um TSMC)

Inside a gate, when we put the transistors together in a CMOS configuration, the individual capacitances can add together.



Then when we put GATES together we get intrinsic, input AND wiring capacitances added together



ASSUME:

All NMOS are minimum sized.
All PMOS are 2x min width, min length.
Unit wiring capacitance is 0.2*Cgmin/um
Cdmin = Cgmin / 4
The highlighted net is 4 um long.

Example:

What is the total capacitance on the highlighted net, in terms of Cgmin?

Cnet = Cinta + Cinb + Cinc +Cwire

= (Cdmin + 2Cdmin) + (Cgmin + 2Cgmin) + (Cgmin + 2Cgmin) + 4*0.2*Cgmin

= 0.75 Cgmin + 6 Cgmin + 0.8 Cgmin

= 7.55 Cgmin

Example:

The data sheets for a standard cell inverter specify that it has an input capacitance of 6 fF and output capacitance of 3fF.
From some clever reverse engineering you've figured out that the PMOS is 2.200um/0.180um and NMOS is 1.180um/0.180 um.
Minimum gate length is 0.18 um, width is 0.22um.

What is Cgmin and Cdmin?

Cin = Cgpmos + Cgnmos

6fF = 10xCgmin + (1180/220) Cgmin

6fF = 18.18 Cgmin

Cgmin = 0.330 fF

Cout = Cint = Cdpmos + Cdnmos

3 fF = 10 Cdmin + (1180/220) Cdmin

Cdmin = 0.165 fF

Conclusion:

When referring to digital gates, we simplify capacitances in terms of an input (Cin) and output/intrinsic capacitance (Cint).

Given relative transistor sizing in a system, you should be able to determine the capacitance on each net in terms of Cgmin and Cdmin.