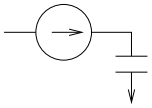
# Delay of a Digital Gate

Fundamentally, In ALL cases: D = C * Vswing/ I



Unit Check:

C [Farad] = Q [coulomb] / V [volt]

I [Amp] = Q [coulomb] / s [sec]

$$D[\text{sec}] = CV/I = \frac{\text{coulomb} * \text{volt} * \text{sec}}{\text{volt} \quad \text{coulomb}}$$

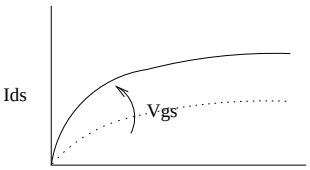
Now then, if only we had a constant current source and a constant capacitance it would be trivial to calculate delay.

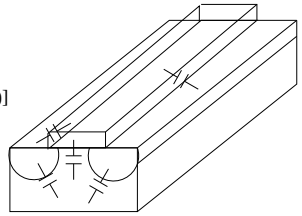
BUT: Current (I) is a nonlinear function of a bunch of variables.

AND, All the capacitances are voltage dependent.

| | |
|---|---|
| Cutoff | Ids = 0 |
| Linear | $Ids = W/L * (ue_{ox} / t_{ox})[(Vgs - Vt)Vds - 0.5\ Vds^2]$ |
| Saturation | $Ids = W/L * (ue_{ox} / t_{ox})\ 0.5*[(Vgs - Vt)^2(1-lambda*Vds)]$ |

Even these are highly simplified models...

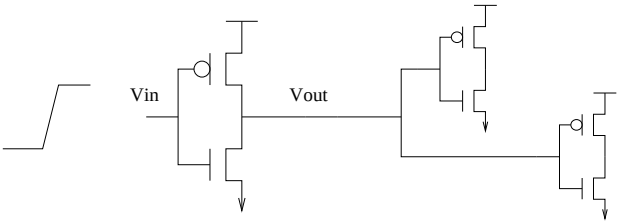


We also have even more complicated models for the voltage dependent capacitances!

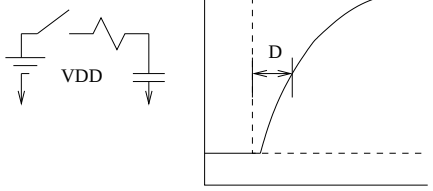
**A SPICE simulator is great for solving all of those detailed equations. We want a simpler way!**

In digital circuits, we are always doing the same thing... Vgs is a step function from 0 to VDD or VDD to 0. What does the output look like?




When we simulate it, we get lucky − the output LOOKS A LOT LIKE a resistor charging a constant capacitor!!!

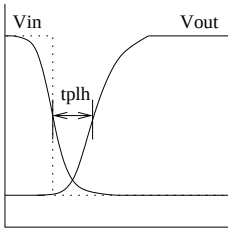
An RC Circuit Charging




From RC circuit theory we know that the delay to reach 1/2 Vout is:

D = 0.69 RC

A CMOS gate switching




In the digital world, this is called the propogation delay from low to how (tplh)

D = CV/I  Recall: R = V/I

If we 'pretend' that there is a constant resistance and capacitance:

tplh = 0.69 * Ctotal * Reffective

So, the question becomes, what are the values for Ctotal and Reffective?

Remember, we introduced these mythical terms to get rid of the complex models. If you REALLY felt the urge you could try to work out Ctotal and Reff but it would be a losing battle. You would need to know the operating mode of the transistors to estimate the instantaneous capacitance and resistance, but the operating modes swing wildly! That's what spice is for.

It is much easier to develop heuristics (rules of thumb) about how the Capacitance and Resistance change with common circuit parameters. You can run a simulation to get the delay (either tphl or tplh), and from there get the effective RC constant of the circuit.