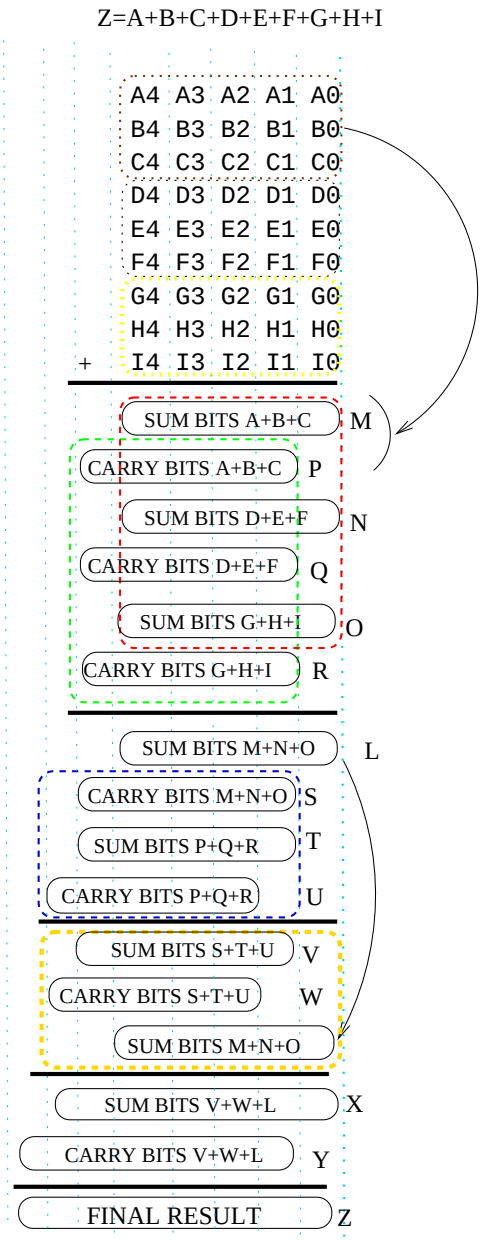

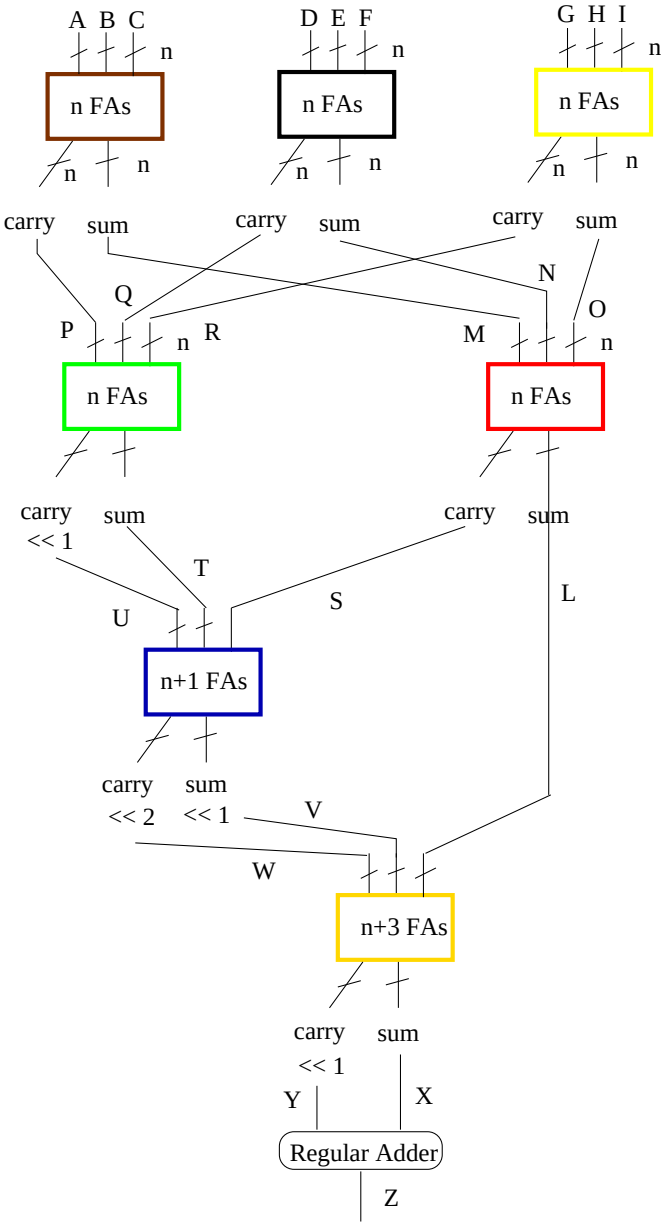

Delay = 4 Full Adders + regular cleanup adder

Multipliers Intro

```
A        1 0 1 1 0   22
*B       0 1 1 0 1   13
carry bits
           0 0 0 0 0
         1 0 1 1 0
       1 0 1 1 0
     1 0 1 1 0
   0 0 0 0 0
 1 0 0 0 1 1 1 1 0   286
```

Output width is width of A + width of B

If the multiplier is implemented with CSA adders it is a 'Wallace Tree'

Signed Multipliers: Sign extend and remove extra logic