Purposes of Testing

Design Testing

Really design verification

Environmental testing

MIL Spec testing.

-55 to +125°C
Radiation hardness

Quality Control tests

Done on samples:
Overvoltage tolerance tests,
Zap (ESD) tests,
High/low temperature tests

Verify Operation

Manufacturing Test

Go No-Go testing

Before Shipping:

Wafer probe test

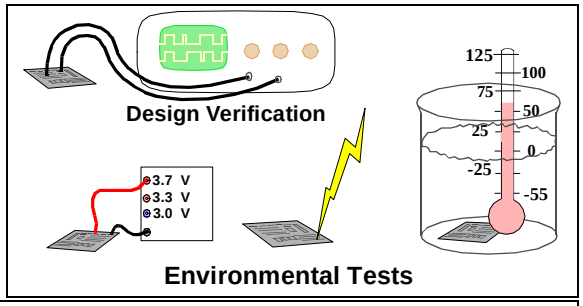
Packaged test

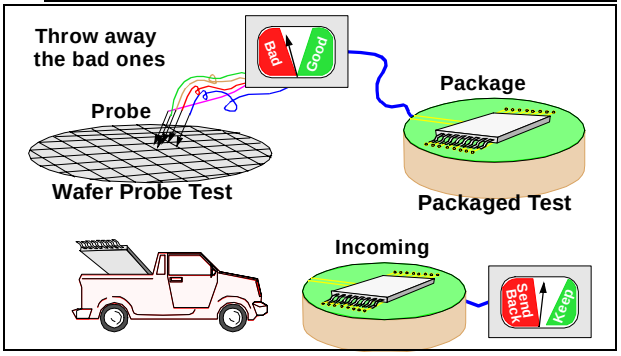
On Receiving:

Incoming test

Diagnostic Testing

Try to locate fault





Testing

The Different Purposes of This Thing Called Testing

Design Testing

This is really *design verification*. To see if the design is correct.

Environmental Testing

MIL Spec Testing.

Test against military standards for temperature (operational testing at -55 and +125°), temperature cycling, vibration, radiation hardness, leakage in package seals, burn in at 135°(24 hrs. inputs low, 24 hrs. inputs high) etc.

Quality Control Tests

Done on samples. High/low temperature tests, operation at high and low V_{DD}, high-voltage spike applied to inputs, lead fatigue (multiple bending). Many of these tests are like mil spec. tests.

Verify Correct Operation, The Main Concern in This Course.

Production Tests

Go No-Go Testing In IC testing we throw away the bad ones

Before Shipping:

- Wafer test are done by probing the chips (die) before sawing up the wafer.
- Package tests are done after placing the die in packages. One uses the same tester with different connections

After Receiving

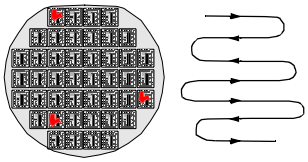
- Incoming inspection by the buyer. Often omitted after buyers learns to trust vendor's testing.

Diagnostic Testing Try to locate fault

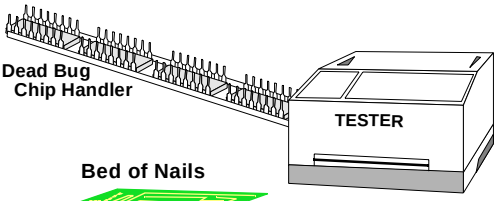
Done for boards as they are repaired. Also to locate cause for frequently seen faults on chips.

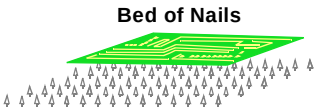
Find Faults Early or Costs Explode

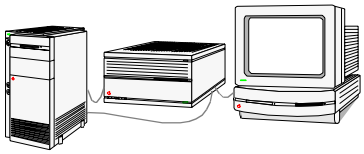
- **Wafer Probe** — $1
  - Step and repeat over wafer
  - Ink bad die
- **After Packaging** — $10
  - Outgoing Inspection
  - Incoming Inspection
    - Shipping damage
    - Don't trust supplier
- **Board Test** — $100
  - Boundary scan
  - Bed of nails
- **System Test** — $1000
  - Complete System Test
  - Customer Acceptance Test
- **Field Repair** — $10000
  - Cost to Fix an Error



Step the probes across the wafer testing each die. Mark the bad ones to be removed after sawing







Costs Increase 10x for each step
The Ten Times Rule

Production Testing; Cost Of Finding A Fault

The wafer probe

The complete wafer is placed on a machine which steps over the individual dies, lowers fine probe wires down on the pin pads and tests the dies.

Package testing

The wafer is sawed up and the dies are mounted in packages. The packages are placed in a handler which inserts them one at a time in the tester. The handler shown was for older dual-in-line packages. It shook the packages with their pins in the air and was called a dead bug handler.

Board testing

It used to be that boards were more accessible that chips, and one could get at their leads with probes. Then boards were tested by placing them on a "bed of nails" which would connect most leads to a tester.

Modern boards have many layers (some up to 13) and it is not possible to get at many of the leads. Also the number of pins would be very large. Try 5000 pins with 5 gm per pin. That is 25 Kg pushing up on the board!

Boundry scan is the new alternative method of board testing which will be described later.

System testing

Testing the complete system

The Ten Times Rule

For every step finding a fault is delayed, the costs increase an order of magnitude.

Production Testers

Typical Tester

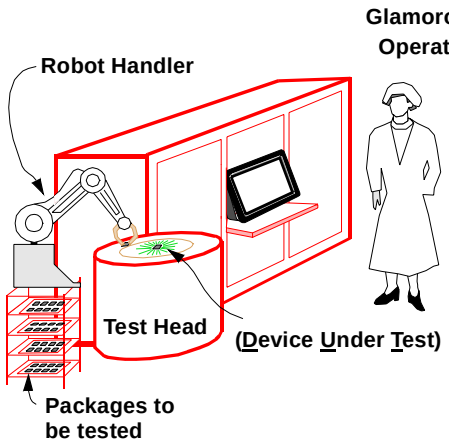
- $2,500K plus
- Robot handlers to load chips
  Likely cost $100K to $500K
- Test time $4.00/min.

Test Head

- 250 pins
- 500 MHz clocking
- 100 ps resolution
- Test 1V to 30V circuits

Test Times/Cost

- Typically $4/min
- Test length of seconds preferred
- Test cost may be 20% of chip cost, 50% not unknown.



Economics of testing

Cost of testers

50$K (small low speed)
up to 10$M (high speed for many pins)

Test heads are the biggest cost.

250 to 1024 pins,

Resolve time to 100ps. Two cm more wire on one pin than another, can cause unacceptable skew.

Clocks of up to 1GHz. Theoretically the tester should be faster than the device under test. Actually many chips exceed their tester speed.[1]

It must test logic levels from -5V up to perhaps 30V. Some common levels are -5.2, 1.1, 3.3, 5, 15.

The tester must deliver millions of test patterns, 200 bits wide. Each pin needs a separate bit.

If it can do this, it can test most digital chips.

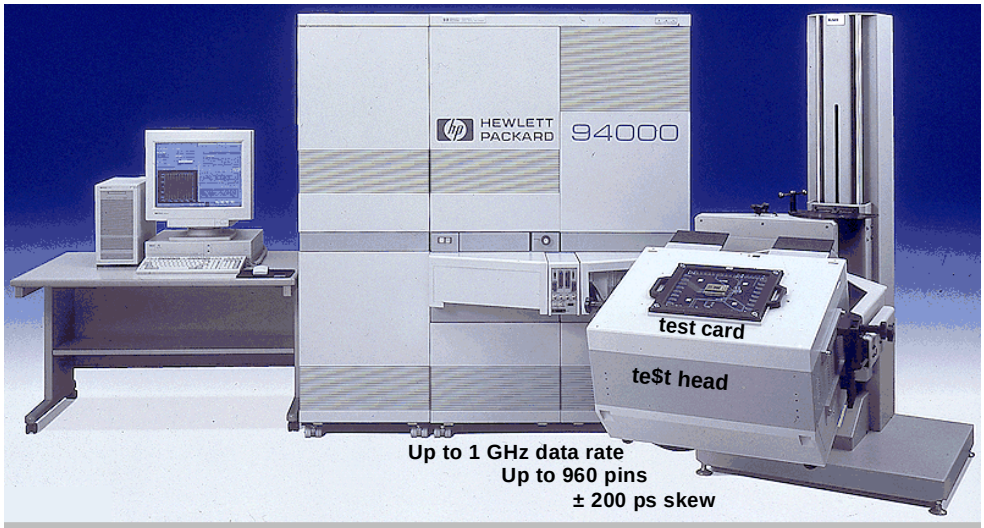
$2500K Tester

maintenance	15%	$375K
space/power/cooling	2%	$50K
interest on capital	10%	$250K
depreciation	20%	$375K
operation	$50/hr	$350K
		$1525K
downtime/unused time	20%	1750hr
program development	15%	1315hr
		5700 hr/year
		$250/hr
		$4/min

Analog /Mixed Signal testers

These are even more expensive.

1. Many fast chips generate their high speed clock internally using a phase-locked loop. To do this they need a very low jitter input clock at a lower frequency.



HP 94000 mixed signal IC test system

A high-end tester

The test head will be fed by a chip handler for packaged chips or a wafer prober for unseparated chips.

A Typical Tester

Agilent 94000 Mixed signal Tester[1]

HP changed it's name to Agilent in 2000.

The most expensive part of the tester is the test head. This one can have:

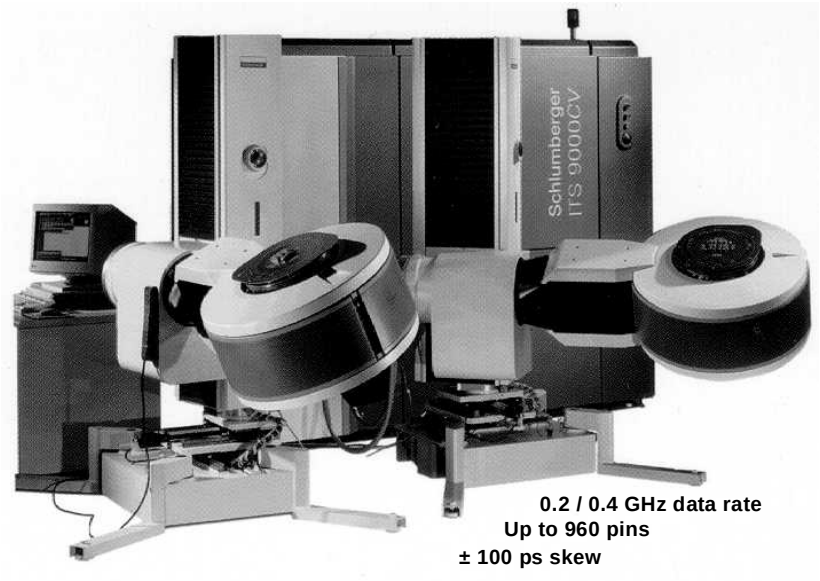
- data rates up to 1 Gb/s,
- a timing accuracy of +/- 200 ps,
- and up to 960 pins.

A digital only tester is the Agilent 83000 VLSI Tester

Its test head can have:

- up to 330 MHz external clock,
- I/O data rate of 660 Mb/s,
- up to 1024 pins,
- up to 8 Mvector of memory (8Meg x 1k bits; need 1 bit per data pin)

1. http://www.ate.agilent.com/ste/products/intelligent_test/SOC_test/descriptions/94000_description.shtml



0.2 / 0.4 GHz data rate
Up to 960 pins
± 100 ps skew

- **Slumberger tester with two test heads**

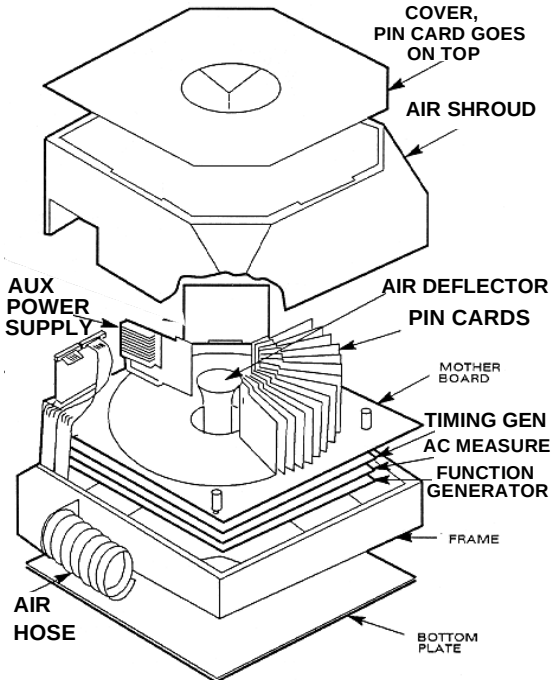
Slumberger testers[1]

System Specification	9000DX High Speed	9000CL High volume
Data Rate	200/400 MHz	100 MHz
Edge Placement Accuracy	± 100ps	± 375ps
High Speed Clock	800 MHz	200 MHz
Pattern Memory	32MV max. (mega vectors)	Up to 16M Vectors
Timing Set	4096 sets	
Digital pin max.	1024 pins	
Algorithmic Pattern Generator	16X, 16Y, 4Z	16X, 16Y
Scan	512, 1024, 2048 Mbit	1.2 GB
IddQ	Ranges (10µA,100µA) 2K stored values	

1. http://www.1.slb.com/semiconductors/socsys/ITS9cv_p.html

Inside the Test Head

- Pin cards placed vertically for close packing beneath pin card
- Air deflector and air hose give much cooling. The pin drivers run HOT.
- Timing generator places data. (Like starts 50% after clock, duration 40% of clock.)
- Function generator does simple calc. (Like increment addresses applied to pins.)
- AC measurements (like rise and fall times on pins).



Test Head[1]

This is the expensive part of the tester.

- It must run at high speed.
- The drivers must be able to handle 1.0V to at least 5.0V
- They drive long cables, high capacitance loads.
- Data pins must all change within a few hundred picoseconds at a rate of several hundred MHz.
-

1. http://www.ece.unh.edu/dal/mtl/testing/ee911tutor/index.html

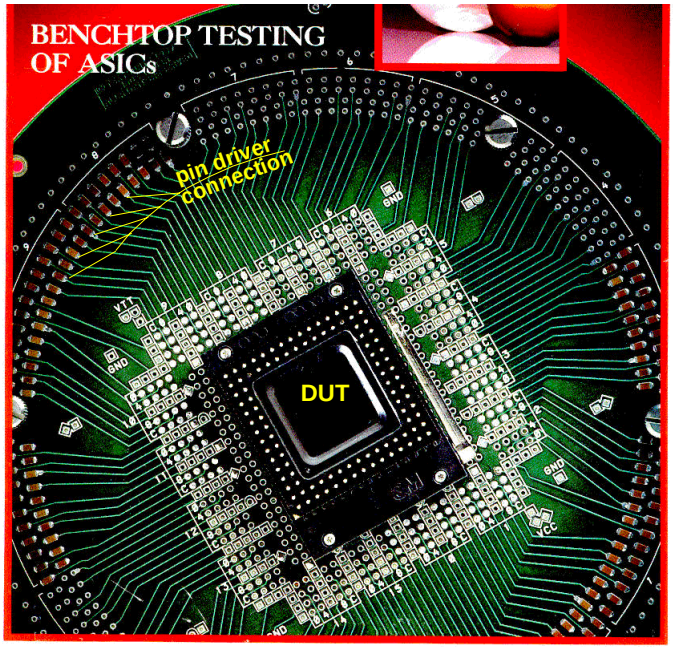
Test Card

The circuit board on the top of the test head. This connects the pin drivers to the DUT (device under test).

Very carefully designed to give equal delay between all chip pins and the tester's pin drivers.

The tester's pin drivers connect near the outer edge of the circle.

This card is made to test packaged chips.



Test Card for a Packaged IC[1]

This IC is already in a package with pins, so it plugs into a socket on this card for testing.

The pin-driver cards on Slide 6 connect to this card near the circumference, and tracks on the card lead in to the pins on the device under test. The tracks must be carefully balanced to be the same length so they do not skew the timing. A few of these connections are identified on the picture.

1. From the cover of the *IEEE Spectrum*, Jan. 1989

Wafer Probe Card

Wafer probe tests are done before the wafer is sawed into die (circuits).

This card contains probe holders, the shaped devices that have a very fine wire at the end.

These probes are carefully lowered to contact the bonding pads on the die.

The wafer is underneath the probe card.

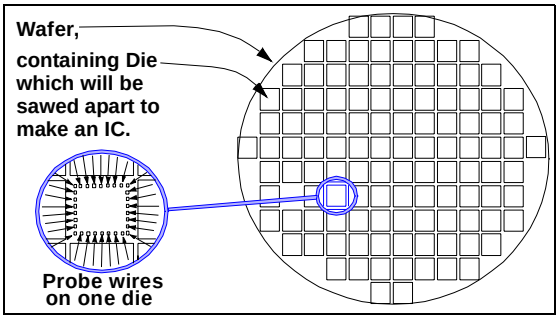
The wafer floating behind the probe card is there by artistic license.

A Wafer Probe Card for Probing Die Before Separating[1]

The prober will move the probe card across the wafer setting the probe wires on the bonding pads around the edge of each die.

The tester will test the die under the probe wires and squirt a drop of paint on the bad die.

The photo shows a wafer floating out behind the probe card, and reflecting multiple colors of light. This was done for glamour rather than an accurate portrayal.



1. The photo was from the cover of *Automatic Test Equipment and Engineering.*

How the Probe Card Fits in the Test Head

Cerprobe wafer probing interface

The mechanism mounts on the test head.

The wafer prober, the part that moves across the die, is on the floor underneath the head.

Test head are supported from the side and rotate to accommodate various probers.

This interface is made to allow relatively rapid probe-card changes.

Attaching the Probe Card to the Automatic Test Equipment (ATE)[1]

Wafer probing establishes a temporary electrical contact between the chip and the automatic test equipment (ATE). This is done to test the performance of the ICs before separation and costly packaging.

This probing is done to very fine mechanical tolerances in what can be a rather rough production floor environment. The probe cards must be immune to bumps and bangs, and yet be changed quickly with a minimum of alignment.

A probing system, which transmits electrical signals to the wafer and analyses the signals upon their return, has three principal components:

1) the ATE test board,
2) the ATE interface assembly, and
3) the probe card to the IC being tested.

The ATE test board is a complex, multi-layer PCB that is mounted directly on the ATE and transfers the test signals back and forth between the ATE and the pogo tower. It is also referred to as a PIB (prober interface board) or a DUT (device under test) board.

The ATE interface assembly typically consists of a spring pin tower, lock-ring, and insert ring. This assembly mechanically connects the ATE with the wafer prober and carries the electrical signals between the ATE and the probe card attached to the wafer prober.

As shown on Slide 6 and Slide 8, the probe card contains the many fine wires which press down on the pads of the IC. These are usually custom made for each IC and are very critical both electrically and mechanically.

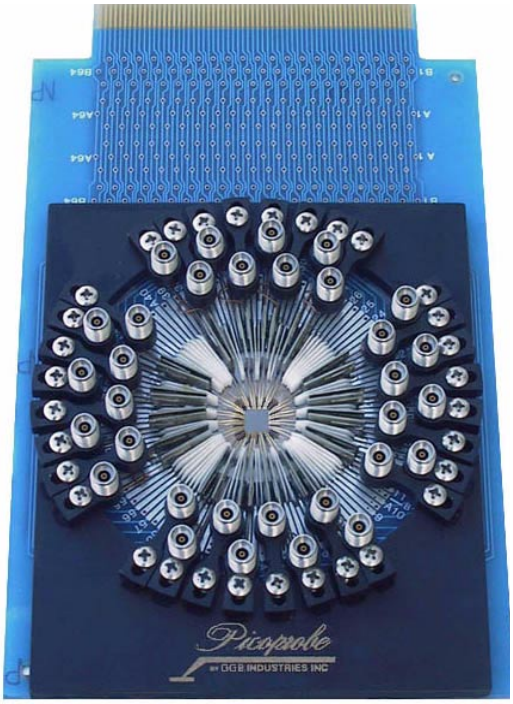
1. http://www.cerprobe.com/CRPB/Solutions/Wafer_Test/default.asp

Probe card with RF connections

This is a mixed signal card. Not pure digital.

The probes that descend to touch the bonding pads are visible in the centre.

The mechanical part of the prober will:
- **place the probe card over the die.**
- **lower the probes to contact the die.**
- **wait while the test is run.**
- **raise the probe card.**
- **move the card over the next die.**
- **lower the card.**
- **. . .**



PicoProbe Card[1]

Wafer Probe

There is a mechanical carriage which very accurately moves the probe card across the die. This must be accurate within a few tens of microns across the area of the wafer. Since it must only probe relatively large I/O pads, not individual lines, it does not have to be accurate to tenths of a micron.

1. http://www.picoprobe.com/pc2.htm

Types of Digital Production Tests

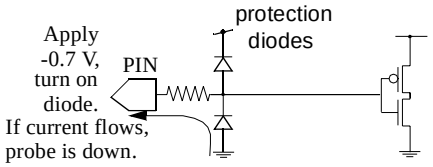
- **Probe Down Test**
  - Tells if pins connection are actually made
  - Check power supply current of chip (Check no internal shorts)
- **DC Parametric Tests**
  - Check input leakage
  - Check output drive when high
  - Check ability to sink current when low
- **AC Parametric Tests**
  - Check output rise and fall times
- **Functional (Logical) Tests**
  - Functional Test Vectors (Special cases designer wants to check
    Example: Does carry chain propagate from x_0 to x_{64}
  - Automatically Generated Tests, usually scan tests for stuck at faults.
  - Delay-fault, stuck open, and other two-step tests.
- **IDDQ Tests**
  - Apply test vectors slowly
    check that quiescent IDD for whole chip is nearly zero.

Types of Tests

Probe-down Test

Probes are rather delicate and easily bent. Also the alignment may not be perfect across the wafer. For these reasons one must check if the probes make proper contact before continuing a test.

The probe-down test sends current through the over-voltage protection diodes connected to the pins.



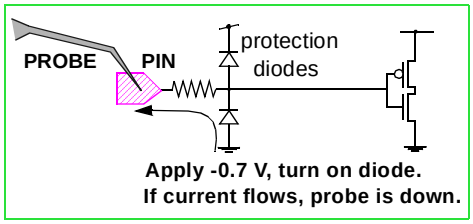
Power Supply Tests

They check that I_{DD} is within limits, i.e.the power leads are not partially or fully open and not partially or fully shorted.

• **Probe Down Test**

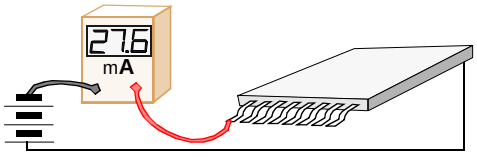
First test done.
Checks that a current can flow through the probe into the die.

It send current through the protection diodes.



Apply V_{CC} and measure current

Check for short circuits and open circuits.

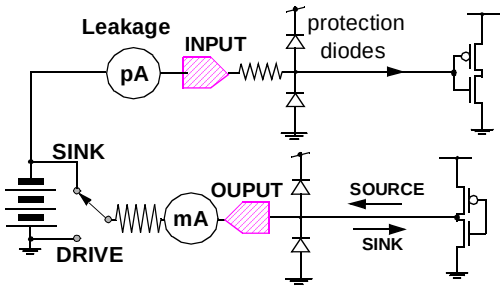


• **DC Parametric Tests**

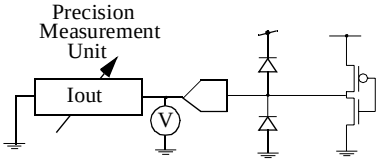
Check input leakage

Check output drive when high

Check ability to sink current when low



DC Parametrics



What is usually done for DC parametrics, is to load the chip outputs with an adjustable current source. This forces the output current to the desired value for measurement. Then the output voltage is checked.

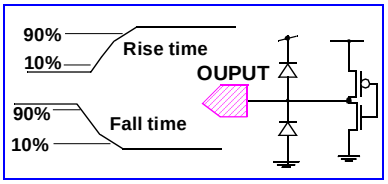
$V_{OH;}$ The output voltage under load when Iout is set to the desired load current for a high output.

V_{OL}; The output voltage under load when Iout is set to the desired load current for a low output.

For CMOS, V_{OH} is very close to V_{DD} and V_{OL} is very close to V_{SS}.

- **AC Parametric Tests**

  Check output rise and fall times



- **Functional (Logical) Tests**

  Functional Test Vectors

  (Special cases designer wants to check

  Example: Do carry chain propagate from x_0 to x_{64}

  Automatically Generated Tests,

  Usually scan tests for stuck at faults.

  Special Tests

  Delay-fault, stuck open, and other two-step tests.

Logical Test

Apply clock
Reset

	(Inputs)	(Expected Outputs)
Apply test vector 1	0 1 1 0 1 ...	0 1 1 0 1 ...
Apply test vector 2	1 1 0 0 1 ...	0 0 0 0 1 ...
Apply test vector 3	0 1 1 1 1 ...	0 1 1 1 1 ...
Apply test vector 4	1 1 1 0 1 ...	1 0 0 0 0 ...
Apply test vector 5	1 0 0 0 1 ...	1 0 1 0 1 ...

- **I_{DDQ} Tests**

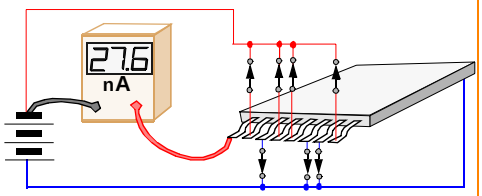
  Disconnect all outputs.

  Apply test vectors slowly.

  Check that quiescent I_{DD} for whole chip is very small.

  Quiescent current can take ms to stabilize.

  Only a few test vectors are done.



Apply slow signal to pins (shown as switched here)

AC Parametric Tests

Rise and fall times can only be done for the output pins.

In some cases clock to output delays can be tested.

For a simple circuit with access to both ends of flip-flops, setup and hold time measurements may be done.

Logic Tests

These are the designers major concern with testing.

Some tests are determined by the designer to be sure certain functions are tested. A designer would like to be sure the data works for FFFF and 0000. Does it work for leap year, and other specific cases which might be missed in automatically generated tests.

Automatic test pattern generators normally generate tests that check the leads on individual gates. They try to propagate a signal from each gate input to the gate output.

Sometimes a gate will appear to give the correct value but may still be defective. If the feedback path in a latch is open, the latch may appear to work because it holds the data temporarily in stray capacitance. However it will lose its data after a few microseconds.

I_{DDQ}

These tests can often find faults that other tests do not. A gate with a partial short, may function correctly in some cases, and not be found with a logic test. However in many cases the short will increase the power supply current.

Measuring I_{DD} after all transients have had time to settle, may show an increased value. It can take hundreds of microseconds for the transients to settle, so one does not have time to apply the millions of test inputs (vectors) that are normally doe for logic tests. Fortunately a large number of the faults can be found with only a few tens of tests.