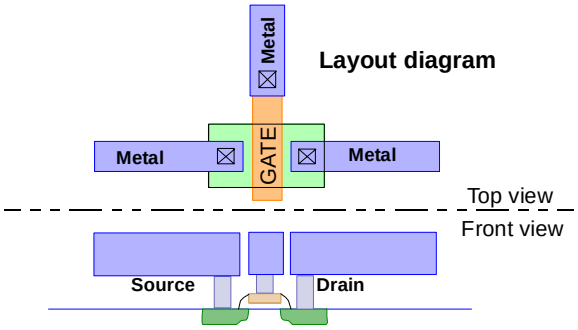
Design Flow

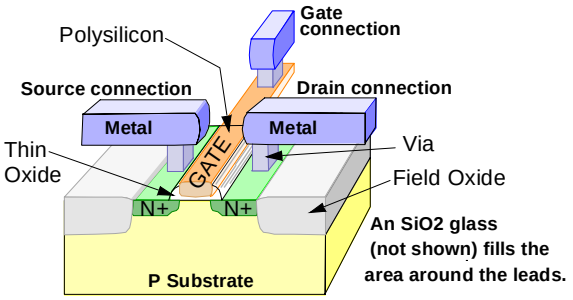
Design Flow

the sequence of design steps with associated software *tools* which one uses to go from the circuit specification to the final *layout diagrams*. (tapeout)

A slightly simplified *layout diagram* for a transistor.



The NMOS transistor *that* would be fabricated from the *layout diagram*



Design Flow ▪

Design Flow Terms

ASIC

Application Specific Integrated Circuit. Almost all ICs are ASICS except micros and memories.

tools

A programs used for one or more of the steps in the design flow.

layout

The diagrams showing what is on each layer (or better, each processing step) in the integrated circuit.

Here one layer (green in the top view) would show where to diffuse an N type dopent into the substrate to construct the source and drain. Another step layer (blue) shows where the first metal layer would be placed.

tapeout

Originally circuit layouts were shipped to the mask maker on magnetic tape. Sending out this tape was the designers last step before he/she fell over from sleep deprivation. The name stuck after FTP replaced magnetic tape.

foundry

A plant for building integrated circuits, or steel castings. In these notes it if the former.

TSMS

Taiwan Semiconductor Manufacturing Company. Is the largest IC foundry service in the world. The 2nd largest, UMC (United Microelectronics Corp), is also in Taiwan. The 3rd largest is IBM, followed by Chartered Semiconductor Manufacturing Pte. of Singapore. (Written in 2003)

Trivia

The smallest feature size in the 2003 manufacturing processes are about:
0.09 micrometers (micron) = 90 nanometers = 900 Angstroms (A°)
The gate oxide in this process is of the order of 20 A° or about 8 molecules.

Design Flow

Design Flow:

- The sequence of steps in designing an *ASIC* (Application Specific Integrated Circuit).
- Most steps use a design *tool* (program)
- Flows change with different processes (Motorola, TSMC, 0.18μm, 0.13μm . . .)
- Flows and tools change between companies.

This flow uses Cadence Design tools supplied by CMC (Canadian Microelectronics Corp.)

Design Flow Steps

Specifcation

System design must often meet standards.

From a standard, the designer creates a model, often in C.

Other system modelling tools are
System C,
Matlab/Simulink,
Cadence's SPW, or
Synopsys' Co-Centric

System-level variegation

Usually done by simulation.

IEEE

802.3 Ethernet
802.5 Token ring
802.6 Metropolitan area networks
802.9 Isochronous LAN
802.11 Wireless LAN
802.14 Cable modem
802.16 Broadband wireless access
802.20 Mobile broadband wireless

MPEG

MPEG-1, Video CD and MP3
MPEG-2, Dig. TV set top boxes & DVD
MPEG-4, Multimedia for web.
MPEG-7, Describe and search multimedia.
MPEG-21 Multimedia framework

Some Standards Groups Important to ASIC Designers

Institute of Electrical & Electronic Engineers (IEEE)

Electronic Industries Association (EIA) and it's subsidiary
JEDEC *Solid State Technology Association* (formerly Joint Electron Device Engineering Council)

The Telecommunications Industry Association (TIA) Standards usually joint with EIA

International Telecommunications Union (ITU) Formerly CCIT.

International Standards Organization/International Electrotechnical Commission (ISO/IEC)
Moving Picture Experts Group (MPEG), its working group on digital audio and video standards
http://www.chiariglione.org/mpeg/

Consumer Electronics Association (CEA)

Japan Electronic and Information Technology Industries Association (JEITA) Consumer products.

Often there are competing standards, for example for cable modems there were originally standards from:

Europe
The Digital Audio-Visual Council (DAVIC),
Digital Video Broadcasting Project (DVB) standard DVB-C
European Telecommunications Standards (ETSI) issued ETC 300 800, from joint DAVIC-DVB work

North America
Multimedia Cable Network Systems (MNCS) a group of manufacturers who produced the
Data Over Cable Services Interface Specifications (DOCSIS) approved by ITU.

International
IEEE 802.14 cable modem standard. This was abandoned in 2000 in favour of DOCSIS.

For a good start on standards organizations try.
http://www.webstart.com/cc/standards.html

RTL Design (Verilog, VHDL)

The Register-Transfer-Level (RTL) sometimes called Behavioural design.

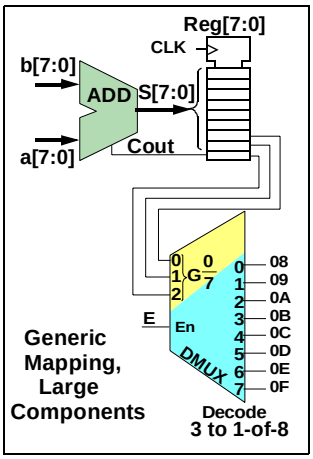
Uses adders, multipliers, counters, memories, finite state machines etc.
Usually described with Verilog or VHDL code.

Converting the system level algorithm to a RTL,
(say converting C to Verilog)
Typically done by manual HDL coding. (but see notes)

Verification by Simulation

Simulate using I/O vectors developed with system-level model.

RTL simulation tools:
Cadence's XL or NC-Verilog,
Synopsys' VCS, or
Mentor's Modelsim.



Synthesis

Generic Mapping

Automatically map RTL (Verilog) description to generic hardware part: muxes, encoders, flipflops, adders & gates.

Unsynthesisable code, unwanted latches and basic synthesis problems are found here.

This mapping is part of tools like:
Synopsys' Design Compiler(DC)
Cadence's Buildgates/PKS.

Synthesis

There are Two Libraries

1. Generic Cells

These are circuit components which are easy to later translate into more specific standard cells.
They are often large scale like adders, muxes, priority encoders and decoders, which are easy to infer from high-level constructs. For example a case statement maps easily into mux. Note however, that there are smaller gates like NAND and FLIP-FLOPs. Generic cells are general logic elements and have no layout, timing or power specifications.

2. Specific Library Cells

These cells are design specifically for a certain process like 0.9µm CMOS at IBM. They have specific layouts, although these are often hidden so the user cannot look at them. They are considered valuable intellectual property and closely guarded. They have timing and power use models which the user can see, usually for a good price. They are what will actually be fabricated.

Direct C->Hardware (2003)

There are firms offering C/C++ or System C direct conversion to Verilog/VHDL

CoCentric SystemC Compiler from C-Level Design (now Synopsys)
Forte Design System,(merger of CynApps, Inc. and Chronology Corporation) Cynthesizer
Frontier (http://www.frontierd.com).
Forge, a Java to Verilog Compile by Lavalogic (now Xilinx)

Constraints

Apply before mapping generic hardware into library cells.

Timing

The synthesizer optimizes circuit to meet time constraints.
Main time constraint is clock period.
Other constraints are delays from pins to flip-flop inputs.

Floorplanning

Below 0.35μm feature size, delay due to interconnect leads becomes more significant than gate-delays.

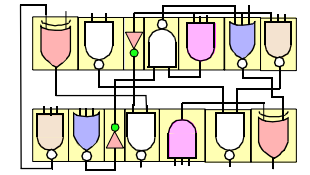
For short delays, cells must be physically close.
Thus, in order to determine whether a design will meet timing requirements, the layout must be known.

Basic floorplanning is done in this step, so that the interconnect delays can be estimated during compilation.

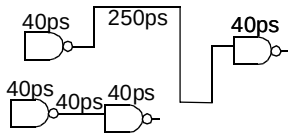
Power Planning

Each cell is connected to power and ground along its edges.
The current through any wire must not exceed some threshold to avoid *electromigration*.

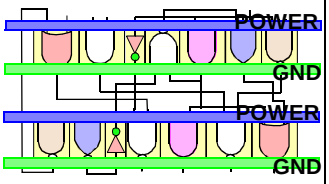
Based on your design's speed, layout, and toggling activity, power rails must be distributed across the design to maintain this limit



Library cells arranged in a chip



Interconnect delay is important

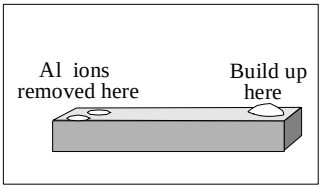


Power Rails

Electromigration

At currents much lower than the wires melting point, they are subject to electromigration.[1]

A direct current in a metal wire running over a long time period causes a transport of metal ions which gradually increase the lines resistance and will eventually cause the wire to break or to short circuit to another wire.



Wires which carry AC and are less susceptible

Rate of electromigration depends on $1/(\text{current density})^2$

In Al a upper current density of 0.1 MegaAmps/cm^2 (1 mA/(μm^2) can be used to determine minimal wire widths

Adding alloying elements (Copper, Tungsten) also helps prevents movement of Al ions.

[1] Large wires have a low surface to volume ratio, and they will melt before electromigration is important. Small wires have a larger relative surface area, and can cool themselves better.

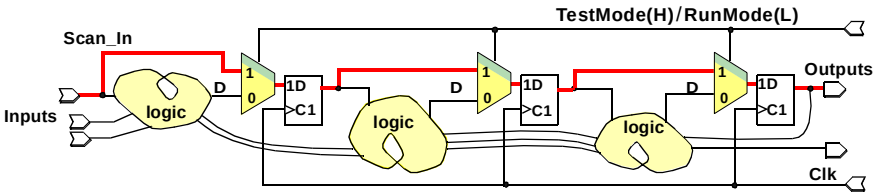
Compiling To Standard Cells

From:
- **the circuit of generic cells,**
- **the clock period and other timing constraints,**
- **the wire delays estimated from the initial layout,**
- **and perhaps the power requirements,**

the synthesizer picks elements from the digital library and logically arranges them to meet timing, area and power constraints.

Scan Insertion

For production testing, all the circuit flip flops can be reconfigured into long shift registers called scan chains.



In *Test Mode*, any desired test signals can be shifted into the flip-flops.

This makes testing much easier.

The test-insertion tool automatically place muxs at all flip-flop inputs. It links them together to form shift registers.

During *RunMode* the circuit is unaffected[1] by the shift registers.

There are test insertion tools in Synopsys' DC, Cadence's PKS,

Test Insertion

Synopsys' latest test insertion and test design tool is *DFT Compiler.*
See also Mentor's *Fastscan.*

Test Vector Generation

Even if you have scan so you can write and read to all the flip-flops, you still need test data, called test vectors, which will exercise and test every gate. These can be tedious to find, but there are programs which do a very good job on this.

This is a good point to generate the test vectors and evaluate how well they test the circuit (coverage). If they cannot test the circuit adequately, one may have to insert some additional test pins or other circuitry.

[1] During run mode the muxs do slow down the circuit slightly.

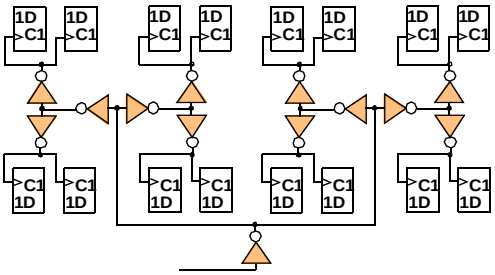
Clock Tree Insertion

Ideally all flipflops receive the clock signal at the same time.

Variations in buffering, loading, and interconnect lengths, skew the clock's arrival.

A clock-tree insertion tool routes the clock lines and places clock buffers to minimize skew.

Some clock tree insertion tools
- Cadence's, CTSGen, Ctgen, and CTPKS.
- Ultima's ClockWise



Balanced Clock Tree

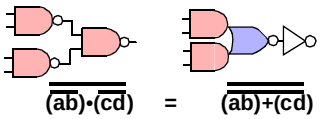
Optimization

After:
placing the cells,
adding scan circuitry and
inserting a clock-tree,

the design may no longer meet timing requirements.

Optimization can:
- restructure logic,
- re-size cells, larger cells are faster.
- vary cell placement

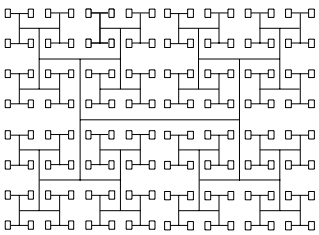
in order to meet timing constraints.



Clock Tree Generation

Skew is the difference in time of the clock edge arrival at different flip-flops

For minimum clock skew, one should have all clock paths travel through the same number of buffers with the same rise and fall times (the same sizes). Also the interconnect lengths to the source should be the same. The circuit shown accomplishes that. It is called an H tree since it is made recursively from H shaped interconnections.



A larger H tree

An overview of clock tree generation is given by Ulf Nordqvist of Linköping University, Sweden, "Clock Tree Generation Beating the clock?," http://www.isy.liu.se/~ulfnor/clk_tree.pdf

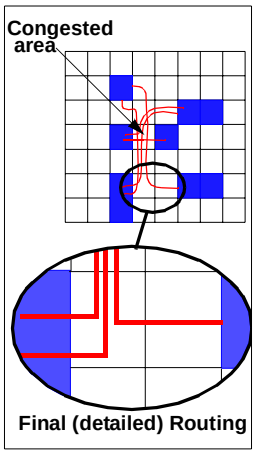
Routing

Initial timing estimates assume routing with no wiring congestion. Actual routes are longer to run around congested regions.

The final routing is performed in two steps:

1. **Global Routing creates a coarse routing map of the design. It finds areas which are highly congested and routes signals around those area. After global routing, retime the design using the improved interconnect lengths.**
2. **Final Routing uses the plan from the global route and lays out the metal tracks and vias to physically connect the cells.**

Two Cadence routers are available - WarpRoute and NanoRoute. Synopsys has Route Compilier.



Parasitic Extraction

Once the detailed routing tracks are inserted, an extraction tool is used to determine the resistance and capacitance of each net.

These tools also find the cross coupling capacitance between two lines These are important for evaluating crosstalk which may couple fast pulses.

Some extraction tools are:
Cadence's (formerly Simplexe's) Fire & Ice
Cadence's HyperExtract
Synopsis' (formerly Avanti`s) Star-RC
Celestry's Nautilus
Mentor's xCalibre

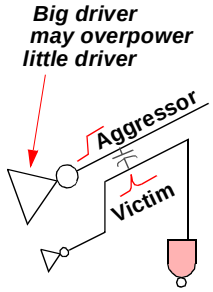
Routers

The Global router places leads through the course boxes called *routing bins* or *gcells*. It limits the number of wires through a cell to avoid congestion, but it does not do the detailed placement of the wires inside the bins. In fact it may slightly overfill some.

The detailed router does the detailed wire layout. It may have to reroute some wires, or it may have to add vias to send the wire to another layer.

Post-Routing In-Place-Optimization

After importing the parasitic information timing is re-evaluated.
If it does not meet constraints, limited fixes can be performed:
- **cell re-sizing,**
- **limited re-routing of a few lines,**
- **via insertion.**



Signal Integrity Fixes

With high interline cross-coupling capacitance, quick transitions on one line can affect the other.

These nets are referred to as *victims* and aggressors.

***Aggressors* are characterized by large drivers and quick transition times.**
***Victims* have weak drivers.**

Signal integrity violations can be divided into two categories:

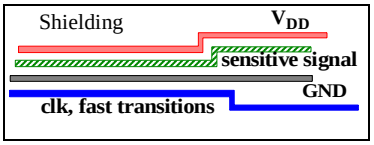
1. **Crosstalk: when a victim and aggressor pair transition at the same time. The victim's edge may speed up (both transition in the same direction), or be delayed. Crosstalk can change both best and worst case timing.**
2. **Glitching: when an aggressor transition causes a logical glitch (or) on the victim.**

A signal integrity tool identifies problem nets for repair.
(Cadence's CeltIC, Synopsis' PrimeTime SI)

To improve integrity:
- **buffers can be inserted,**
- **nets can be re-routed, or**
- **shielding (a grounded line) can be inserted between the offending nets.**

Fixes

Any line which will not budge when hit by a glitch will work for shielding. V_{DD} or GND are equally good.



Reference on minimum density and antenna rules (Peter Y. K. Cheung, Imperial College)
http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/design%20rules/add-rules.html

minimum density, antenna rules, optical proximity, phase-shift masks. (Ron Ho, Stanford)
mos.stanford.edu/papers/DFMandDSMweb.pp

After any fixes

Extraction is re-done

Timing must be re-verified.

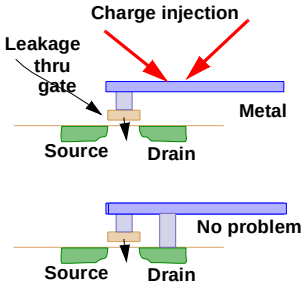
Physical Checks

Once timing closure has been assured, various physical checks are carried out.

Antenna Check

Plasma etching deposits a charge on metal lines.
Source/drain connections dissipate this charge.
Even gate leakage will drain a small metal line.
If the dissipation is too slow the voltage increase will damage transistor gates.

Metal lines that cause this are said to have antenna violation.
To prevent this, leakage diodes can be added,
or long metal traces on a single layer can be prevented.



Layout vs. Schematic (LVS)

The LVS tool extracts the connectivity information (circuit) from the routed layout

It compares this with the original logical netlist (verilog circuit).

LVS locates any errors introduced during the layout ,
or by postsynthesis hand fixes of the design.

Tools to perform for LVS:
- Cadence's Assura (formerly Diva and Dracula)
- and Mentor's Calibre.

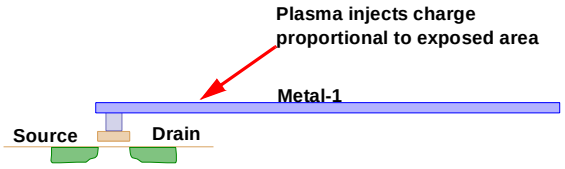
Antenna Violation

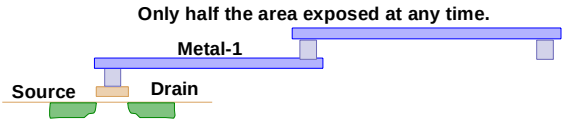
Plasma etching of the layers injects charge on exposed metal areas. This charge must leak through the gates or it builds up as V=Q/C.

The gate area/exposed metal area must be kept under 1/1000 to avoid gate-oxide damage.

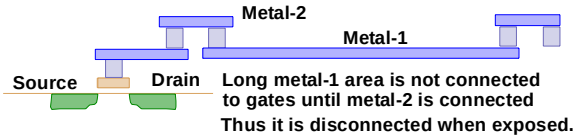
Reversed biased diodes have enough leakage to drain the charge, but they add capacitance and slow down the circuit.

Vias to another layer can also solve the problem as shown.

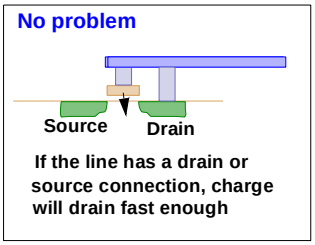




Metal-1 is covered by SiO2 when metal-2 is exposed to plasm. Meta-2 does not exist when metal-1 is exposed.



Long metal-1 area is not connected to gates until metal-2 is connected
Thus it is disconnected when exposed.



If the line has a drain or source connection, charge will drain fast enough

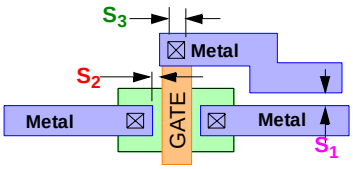
A typical violation requires metal area greater than 1000 times gate area

Design Rule Checking (DRC)

Design rules check validates the design spacing and geometry.

Each process has many design rules:

- minimum metal to metal spacing (S_1).
- minimum contact-to-gate spacing (S_2).
- standard contact size (S_3).
- . . .



The same tools used for LVS are used for DRC, i.e. Assura and Calibre.

Tapeout for Digital Circuits

The wiring data is collected into layers polysilicon, metal-1, metal-2, ...

This is made into a GDSII file.

This data is sent to an agent (for Carleton CMC)

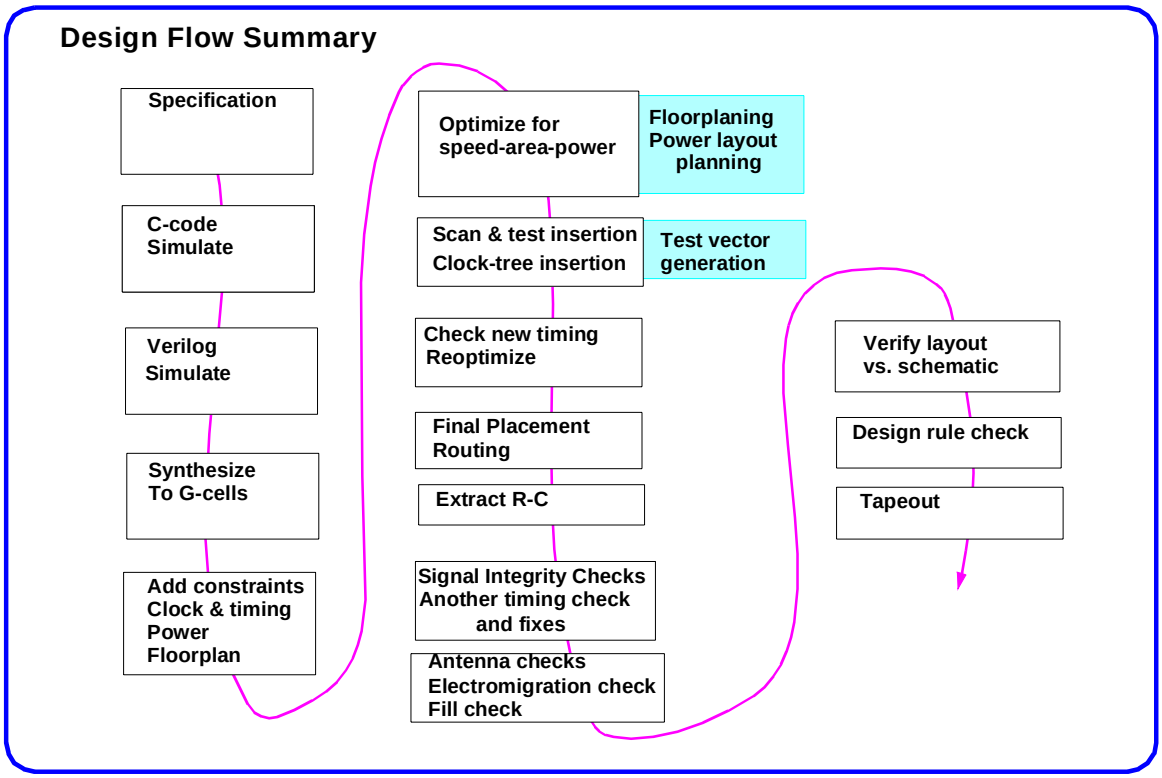
- **They insert the layouts for the standard cells. We are not allowed to see them.**
- **They run a final DRC (design rule check) with the cells layouts in place.**
- **They ship the final design to the foundry.**

GDSII

A long standing, almost universally used, format for transferring IC physical layout from design tools to mask fabricators. It was developed by GE/Calma for transferring 2D graphical design data to their plotters.

GDSII format is a binary format, but machine independent. Number must be converted from GDSII definitions into machine representation. The instructions define layers, each representing a fabrication mask, defined by multiple polygons.

▪ Design Flow ▪


Design Flow Summary
Specification
C-code Simulate
Verilog Simulate
Synthesize To G-cells
Add constraints Clock & timing Power Floorplan
Optimize for speed-area-power
Floorplaning Power layout planning
Scan & test insertion Clock-tree insertion
Test vector generation
Check new timing Reoptimize
Final Placement Routing
Extract R-C
Signal Integrity Checks Another timing check and fixes
Antenna checks Electromigration check Fill check
Verify layout vs. schematic
Design rule check
Tapeout