Abstract—A circuit technique for integrating built-in complex finite-impulse-response (FIR) and infinite-impulse-response (IIR) filtering functions into operation of a subsampler is presented. Based on integrative multiple sampling in the charge domain, the complex FIR filtering function of the sampler provides internal anti-aliasing and image band suppression prior to quadrature downconversion by subsampling. The complex IIR filtering function, taking place at the output sampling rate of the sampler, performs further first-order channel selection filtering on the downconverted signal. An example 50-MHz IF-sampler implementation in 0.8-μm BiCMOS demonstrating the feasibility of the technique is presented in the paper.

Index Terms—Charge domain, complex filters, quadrature downconversion, radio receivers, subsampling.

I. INTRODUCTION

Increasing radio receiver integration level has been under intensive research for over a decade. The well-known advantages of increased receiver integration degree lie in lower manufacturing costs due to reduced need for external discrete components and also, with the advent of dense high-μf CMOS processes, in system-level integration of both transceiver and digital baseband functions into system-on-chip solutions. Several new architectural solutions, e.g., [1], have been presented to overcome the problems associated with integration of the traditional heterodyne receiver. Another, a very straightforward solution for increasing the receiver integration level is to transfer signal sampling and analog-to-digital (A/D) interface from baseband to higher frequencies, i.e., to a high IF or optimally directly to RF, and to use a high-resolution A/D converter to enable further signal processing in the digital domain with greater digital word lengths [2]. However, as a drawback, this not only imposes demanding requirements for linearity and noise performance of the converter, but also tends to increase total power dissipation of the receiver.

To allow the operation of a high-speed discrete-time A/D converter at IF with reduced resolution, an analog RF circuitry preceding it has to perform at least three signal processing operations: downconversion, filtering, and sampling. A subsampling mixer can perform the tasks of signal downconversion and sample-and-hold operation simultaneously. However, simple subsampling downconverters lack the filtering properties required to suppress unwanted interfering signals and wide-band noise aliasing on top of the wanted signal in the subsampling process. On the other hand, integration of a steep continuous-time bandpass anti-aliasing filter in front of the sampler is difficult at high frequencies. Furthermore, realization of a narrow-band channel selection filter operating at a high sampling frequency in order to attenuate strong interferers increasing dynamic range requirements of the A/D converter can be difficult with conventional switched-capacitor (SC) filter design techniques.

This paper presents an approach for combining finite-impulse-response (FIR) anti-aliasing and image rejection filtering, quadrature (I/Q) downconversion by subsampling, and high-Q-value infinite-impulse-response (IIR) channel selection filtering into one functional sampler block. The complex FIR filtering function is embedded into the subsampling operation by integrating at a high rate several successive weighted current samples into sets of sampling capacitors, which are read out at the low output subsampling rate. The FIR filtering response provides built-in anti-aliasing suppression for the undesirable aliases of the output sampling frequency and also attenuates the image signal band prior to I/Q downconversion resulting from subsampling. The SC IIR filtering operation, based on charge sharing between the quadrature channels, takes place at the output sampling rate of the FIR stage and further increases selectivity of the sampler by providing a complex discrete-time first-order filtering response. An example BiCMOS FIR/IIR sampler realization for I/Q downconversion of a near-50 MHz IF signal to a low IF of 14.5 kHz presented in the paper shows image band rejection (IMR) of more than 44 dB on the 26.3-kHz 3-dB bandwidth of the circuit. In Section II of this paper, the operation principle of the charge-domain FIR/IIR sampler is described. The example IF-sampler realization is described in detail in Section III, and the measured results of the implemented circuit are shown in Section IV. Finally, conclusions are given in Section V.

II. CHARGE-DOMAIN FIR/IIR SAMPLER

A. Charge-Domain FIR Sampling Operation

The integrative multiple charge-domain sampling technique integrates both continuous-time and complex discrete-time filtering functions into operation of the FIR/IIR sampler, allowing bandpass input signal quadrature downconversion by subsampling with high dynamic range. Fig. 1 presents the simplified schematic diagram and the timing diagram for one output sampling cycle of a pseudodifferential active integrator-based realization of the charge-domain sampler. Note that a fully differen-
Fig. 1. Principle of the pseudodifferential complex charge-domain FIR sampler.

tial sampler implementation is also possible to obtain improved common-mode signal rejection.

In the charge-domain FIR sampling operation an input voltage is first transformed into a corresponding current in a transconductance ($G_m$) cell with a transconductance gain $G_m$. The output current of the cell is alternately integrated into four negative feedback-connected real ($I$) and imaginary ($Q$) channel sampling capacitors $C_s$ in four adjacent clock phases. The length of each integration phase is $T_i$, which is also equal to time delay between the adjacent integration phases. The process of acquiring the four quadrature charge samples repeats itself according to the timing diagram of Fig. 1. During the output sampling period $T_s$ of the sampler, the charge is accumulated into each of the four sampling capacitors $N/4$ times, thus yielding a total number of $N$ accumulated charge samples. After the charge accumulation cycle, the four quadrature outputs of the sampler are read at the output sampling rate $f_s = 1/T_s$. The integration of several current samples at a high rate during a longer output sampling period results in inherent subsampling operation from the bandpass input signal point of view. As the location of the sampler’s output signal spectrum is fully determined by the output sampling rate, a charge-domain sampler with a bandpass FIR filtering response can be used for IF/RF signal downconversion by subsampling or decimation [3], [4]. Note that in a stand-alone charge-domain FIR an additional sampling capacitor discharge phase is required after the charge accumulation cycle to obtain the correct FIR filtering response. However, due to a leaky integrator-type operation of the FIR/IIR sampler’s IIR filtering function, the additional reset phase can be omitted.

The multiple integrative charge-domain sampling operation results in two distinct filtering responses: the integration of input current within a determinate time window produces a continuous-time $\sin(\chi)/\chi$-type low-pass filtering response, whereas the multiple weighted accumulation of charge into the four sampling capacitors of the two quadrature channels yields a discrete-time complex FIR filtering function. Assuming that the active integrator unit performs ideal integration of the input current, the continuous-time amplitude transfer function resulting from the gated integration can be expressed as

$$H_{\text{sinc}}(f) = \frac{G_m}{C_s} \cdot \frac{\sin(\pi f T_i)}{\pi f}.$$  (1)

Fig. 2(a) depicts an ideal amplitude response of a charge-domain sampler resulting from the gated integration according to (1). The typical circuit parameters used in the figure are $C_s = 15 \, \text{pF}$, $G_m = 0.5 \, \text{mS}$, and $T_i = 1/(200 \, \text{MHz}) = 5 \, \text{ns}$. For comparison, the amplitude response of a simple voltage-domain sampler with an equal voltage gain, and an equal 3 dB bandwidth limitation due to the RC time constant of a sampling switch resistance and sampling capacitance is also shown. Fig. 2(a) shows that the gated integration of current produces zeros on multiples of inverse of the integration period length $1/T_i = 200 \, \text{MHz}$, ideally attenuating high-frequency components at the input of the charge-domain sampler more than the RC low-pass filter in the simple voltage-sampling circuit. The ideal 3 dB bandwidth of the low-pass sinc response is approximately $f_{3\text{dB}} \approx 0.44/T_i = 88 \, \text{MHz}$.

The discrete-time FIR filtering response of the sampler arises from the multiple accumulation of charge into the four sampling capacitors. The alternate integration of input current into the positive and negative branches of both quadrature channels results in repeating sequences of sampling weights $h_{kn} = \{+1, 0, -1, 0\}$ for the $I$ channel and $h_{kn} = \{0, +j, 0, -j\}$ for the $Q$ channel. The constant time delays of length $T_i$ between the adjacent integrated current samples correspond to the unit time delays required in the FIR filtering operation, whereas the four sampling capacitors act as memory elements producing a sum of the delayed and weighted samples. With this information, the $z$-domain transfer function of the complex FIR filtering response embedded into the operation of the sampler can be derived as

$$H_{\text{FIR}}(z) = \sum_{k=0}^{N-1} j^k z^{-k} = \frac{1 - z^{-N}}{1 - j^k z^{-1}} = e^{j2\pi f T_f}$$  (2)

where $N$ is the total number of integrated current samples, i.e., the length of the FIR filter impulse response, and $T_f = T_i = 1/f_{3\text{dB,FIR}}$ is the time delay between the adjacent integrated charge samples, i.e., the sampling period of the FIR filter. The filtering response of (2) can be recognized as a discrete-time complex first-order sinc function, also known as a temporary moving average filtering operation. Note that the length of the integration period $T_i$ does not necessarily have to be equal to the effective sampling period $T_f$ of the sampler’s built-in FIR filter, which allows separate control of both filtering functions’ properties.

An ideal amplitude response of the built-in complex sinc filtering function of the charge-domain FIR sampler is presented in Fig. 2(b) for two different FIR tap counts, $N = 4$ and $N = 8$.
at a sampling frequency $f_{s,FIR} = 200 \text{ MHz}$. The center frequency of the filter, and hence the targeted input frequency, is located at $f_c = f_{s,FIR} / 4 = 50 \text{ MHz}$. As with conventional discrete-time filters, the passband of the charge-domain sampler’s FIR filter is repeated at intervals of its sampling frequency. The first-order sinc response produces zeros on integer multiples of frequency $f_{s,FIR}/N$ apart from the center frequency $f_c$ and its repetitions. A notch at $-f_c = -50 \text{ MHz}$ ideally suppresses the negative (image band) frequencies prior to the actual output subsampling operation allowing the sampler to be used for quadrature downconversion.

By sampling the output of the charge-domain sampler at a rate $f_s = f_{s,FIR}/N$, the zeros of the sampler’s FIR response are located on top of all multiples of the output sampling frequency apart from $f_{s,FIR}$, i.e., on top of all unwanted aliasing frequencies, providing a built-in anti-aliasing filtering effect on a narrow bandwidth. The optimal selection of the FIR filter tap count $N$ and thus the output subsampling ratio comprises several trade-offs. Increasing the number of integrated current samples during the output sampling period narrows the bandwidth of the FIR filter and has an averaging effect on both the aliasing wide-band noise of the front-end [5] as well as on the noise resulting from uncorrelated timing jitter in the clock signals controlling the integration periods [6], hence allowing the use of a larger output subsampling ratio. In principle, in a radio receiver it is advantageous to use a relatively large subsampling ratio in the high-frequency charge-domain sampler to decrease the sampling frequency, and hence the power dissipation, of discrete-time signal processing blocks following it. However, as Fig. 2(b) shows, by increasing $N$ the number of unwanted aliasing frequency channels is simultaneously increased and the built-in anti-aliasing attenuation provided by notches of the FIR filter around the aliases is smaller for a given fixed signal bandwidth. In addition, utilizing a smaller $N$ and hence a higher subsampling ratio allows the use of a more broad-band additional anti-aliasing filter possibly required in front of the sampler.

Besides the elementary quadrature sampler of Fig. 1, the selectivity and built-in anti-aliasing rejection of a charge-domain FIR sampler can be improved at the cost of increased power consumption and circuit area. A brute-force method is to increase the tap count $N$ of the sampler with a first-order sinc function for a fixed output sampling rate by using pipelined and time-interleaved sampling operation, in which several parallel sampler units are each used to accumulate the $N$ charge samples in a time-interleaved manner. Ideally, doubling the number of pipelined sampling stages doubles $N$ for a fixed output sampling rate, resulting in increased selectivity and embedded anti-aliasing suppression. Another possibility is to integrate a more selective FIR filtering function into the charge-domain sampling process, e.g., by using $\Delta\Sigma$ impulse response quantization [7]. It should also be noted that the elementary first-order sinc response of the presented FIR sampler has a fairly limited image rejection capability, which depends on the signal bandwidth in relation to the sampler’s center frequency. In addition to increasing the passband selectivity, integrating an advanced complex FIR filtering function into the charge-domain sampling operation would allow improvement of the image rejection.

Fig. 2(c) shows the total ideal complex amplitude responses of the charge-domain sampler with a sinc-type FIR function for the two FIR filter tap counts ($N = 4/8$). The continuous-time low-pass sinc response due to gated current integration attenuates the nearest unwanted passband of the FIR response of the sampler at $-150 \text{ MHz}$ by more than 10 dB. The multiple integration of IF current increases the sampler’s voltage gain at the passband to $\sqrt{2G_m NT_i}/(\pi C_n)$. Worth noticing is that the passband gain of the sinc-type FIR sampler can be relatively high for a large $N$. The gain can be decreased by increasing the size of the sampling capacitors. Scaling down the gain of the sampler’s back-end reduces output swing and distortion caused by the active integrator stages, making the front-end $G_m$ cell typically the main source of nonlinearity in the circuit. As increasing the sampling capacitors also decreases the output noise floor, by selecting the sampling capacitance to be sufficiently large, the output dynamic range of the charge-domain FIR sam-

Fig. 2. FIR sampler magnitude responses. (a) Low-pass sinc response. (b) Complex FIR responses. (c) Combined responses.
The built-in continuous-time sinc and discrete-time FIR filtering functions of the charge-domain sampler effectively limit the input bandwidth of the sampler thus suppressing wide-band input noise and relieving requirements for additional anti-aliasing filters when used in a radio receiver chain. However, the selectivity provided solely by the presented sampler’s elementary FIR operation is fairly limited and hence subsequent discrete-time filtering sections are needed for channel selection. The operation of the charge-domain FIR sampler can be further extended to complex first-order IIR channel selection filtering simply by adding one additional switched capacitor into each quadrature branch of the sampler as shown in Fig. 3.

The four charges $Q_{\text{rep}}(nT_s), Q_{\text{ren}}(nT_s), Q_{\text{imp}}(nT_s)$, and $Q_{\text{inn}}(nT_s)$ are accumulated into the sampling capacitors of the four pseudodifferential output branches by the charge-domain FIR sampler presented previously. Besides the fixed integrating capacitors $C_B$ continuously accumulating the input charge, the active integrator stages each have additional capacitors $C_a$ connected by switch matrices in parallel with the capacitors $C_B$ to the negative feedback loop. The purpose of the switch matrices is to rotate the capacitors $C_a$ from one quadrature branch to another at sampling instants $t = nT_s$, where $T_s = NT_i$ is the output sampling period of the charge-domain FIR sampler. For
example, with the rotation direction shown in Fig. 3, the capacitor \( C_a \) connected between nodes \( q_\text{rep} \) and \( v_\text{rep} \) at the end of the previous sampling period is connected between nodes \( q_\text{imp} \) and \( v_\text{imp} \) at the end of the next period. Neglecting opamp nonidealities, the ideal output voltage at node \( V_\text{imp} \) at the end of a sampling interval at time \( t = nT_s = nT \) can be written as

\[
V_\text{imp}(nT) = \frac{C_b V_\text{imp}[(n-1)T] + C_a V_\text{rep}[(n-1)T] + Q_\text{imp}(nT)}{C_a + C_b},
\]

(3)

Similar time-domain expressions can be derived for the other four outputs. By defining the \( z \)-transform of the complex input charge of the sampler as \( Q_\text{inc}(z) = Q_\text{inc}(z') + j \cdot Q_\text{inc}(z') \) and the \( z \)-domain complex output voltage as \( V_\text{out}(z) = V_\text{out}(z') + j \cdot V_\text{out}(z') \), the complex-valued transfer function of the recursive built-in filtering operation can be derived as

\[
H(z) = \frac{V_\text{out}(z)}{Q_\text{inc}(z)} = \frac{K}{1 - (\alpha + j\beta)z^{-1}} = e^{j2\pi f_0 T_s}.
\]

(4)

where \( K = 1/(C_a + C_b), \alpha = C_b/(C_a + C_b) \), and \( \beta = C_a/(C_a + C_b) \). Equation (4) shows that the charge sharing process between the \( I \) and \( Q \) channel samples due to rotation of the capacitors \( C_a \) results in a first-order complex bandpass IIR filtering operation taking place at the output sub-sampling rate \( f_s = 1/T_s \) of the charge-domain FIR sampler. The pole location of the complex IIR-type filter is determined by the capacitor value ratios \( \alpha \) and \( \beta \), which are dependent on each other by a constraint \( \alpha + \beta = 1 \). The center frequency of the IIR filter is located at

\[
f_0 = \frac{f_s}{2\pi} \arctan\left(\frac{\beta}{\alpha}\right).
\]

(5)

Equation (5) indicates that similarly to conventional SC filters, the accuracy of the presented sampler’s IIR filtering response is determined merely by the sampling clock frequency and the capacitance ratio.

Fig. 4 shows example amplitude responses of the sampler’s complex IIR filter for different capacitance ratio values \( \alpha \) and \( \beta \). The gain factor \( K \) in (4), which describes the gain from the input charge to the output voltage, is usually taken into account in the transfer function of the sampler’s FIR function and is therefore normalized to unity in the figure.

It can be seen that when \( \alpha \) equals \( \beta \), the pole of the filter is located farthest away from unit circle resulting in the lowest \( Q \) value and thus the worst selectivity, i.e., the widest 3 dB bandwidth. As \( \alpha \) increases, the pole moves closer to unit circle on real axis, increasing both selectivity of the filter and passband gain, which equals to \( 1/(1 - \sqrt{\alpha^2 + \beta^2}) \). Equivalently an increase in \( \beta \) moves the pole toward unit circle on imaginary axis. From a practical point of view, decreasing the size of the rotating capacitor, and hence the value of \( \beta \), is equivalent to transferring a smaller charge from the \( I \) channel to the \( Q \) channel and vice versa. As a special case, the complex bandpass filtering operation of the IIR filter can be restricted to real-valued low-pass filtering by transferring a “zero charge” from one quadrature channel to another. In practice, this can be realized by periodically rotating a discharged capacitor \( C_a \) into each of the four quadrature branches [4]. An example amplitude response of such filter for \( \alpha = 0.8 \) is also shown in Fig. 4.

The passbands of the sampler’s IIR filter are repeated at intervals of its sampling frequency \( f_s \pm k \cdot f_s \). In addition to providing built-in anti-aliasing filtering for the unwanted multiples of output subsampling rate at the high input frequency, the FIR response of the charge-domain sampler also attenuates the repeating passbands of the IIR filter. Fig. 5 illustrates two example combined gain-normalized amplitude responses of a sampler with complex FIR and IIR filtering functions for negative and positive frequencies around the center frequency of the FIR sampler. In the figure, the FIR tap count and sampling rate are \( N = 16 \) and \( f_s \text{FIR} = 200 \text{ MHz} \), respectively. Fig. 5 shows that the zeros of the sampler’s FIR filter are located almost on top of undesirable repeating passbands of the IIR filter apart from the sampler center frequency at \( f_c = 50 \text{ MHz} \). As \( \alpha \) increases, the attenuation for the unwanted passbands, including the image band around \( -f_c \), grows. If the IIR filter is implemented as a real-valued low-pass filter (\( \beta = 0 \)), the notches of the sampler’s
sinc-type FIR response ideally perfectly attenuate the unwanted passbands yielding a maximal built-in anti-aliasing suppression for a given sampler FIR tap count.

It should be noted that although Fig. 3 presents the principle of an active integrator-based realization of the one-pole IIR filter, the opamps are not needed in the actual charge transfer process of the filter and hence a passive realization is also possible. However, similarly to $G_m$-C OTA filters [8], for operation at IF, an active integrator-based sampler realization may be preferred due to its inherent insensitivity to the finite output impedance of the $G_m$ cell and enhanced overall linearity.

III. CIRCUIT-LEVEL BICMOS REALIZATION

To demonstrate the feasibility of the presented sampling technique, a test chip for a charge-domain IF-sampler with built-in FIR and IIR functions was realized in a 0.8-μm BiCMOS process. The targeted IF input frequency of the FIR sampler is $f_c = 50$ MHz, corresponding to an equivalent complex FIR filter operating frequency of $f_{f_s,FIR} = 200$ MHz. The output subsampling rate, equal to the sampling frequency of the complex bandpass IIR filter, is $f_s = f_{f_s,FIR}/192 \approx 1.042$ MHz. The active area of the chip core is 0.7 mm$^2$ while the total power consumption is 85 mW from a single 5-V supply. The structure of the realized test circuit is presented in Fig. 6.

For clarity, only the $I$ channel circuitry is shown; the $Q$ channel circuitry is identical to the $I$ channel circuitry.

In the operation of the circuit four current-biased nMOS sampling switches alternately divert the output current of the front-end $G_m$ cell in four quadrature phases into the feedback-connected sampling capacitors forming the pseudodifferential quadrature branches of the sampler. The IF input current is integrated in total 192 times into the four sampling capacitors during the output sampling period, producing a 192-tap complex sinc-type FIR filtering function embedded into the operation of the sampler. Each integrator stage contains a 2.48 pF rotating capacitor connected by pMOS switch matrices in parallel with a fixed 28.1 pF capacitor, giving feedback ratios $\alpha \approx 0.92$ and $\beta \approx 0.08$ for the IIR filter. The rotation direction of the 2.48 pF capacitor in the test circuit is opposite to the principle circuit of Fig. 3, resulting in an IIR filter center frequency of $f_0 \approx -14.6$ kHz, which corresponds to an IF input of 49.985 MHz.

The opamps used in the circuit are standard two-stage Miller-compensated BiCMOS amplifiers with nMOS input differential pairs, and emitter follower buffers for measurement purposes. The simulated DC gain and unity-gain frequency of the opamp are 83 dB and 209 MHz, respectively. The average voltage level of the pseudodifferential outputs ($V_{rep}/V_{ren}$) is measured by resistors $R_{av}$ and compared to a reference bias voltage of 2.5 V.

![Simplified schematic of the realized test circuit.](image-url)
by a common-mode feedback (CMFB) amplifier \( A_{cm} \), which controls the pMOS current sources providing bias current and adjusting the output DC level of the transconductor. The same negative feedback loop also controls the output common-mode level of the opamps.

The schematic diagram of the used high-frequency BiCMOS transconductance element is presented in Fig. 7. The \( G_m \) cell utilizes local negative feedback to decrease emitter impedance of the common base-connected NPN transistor \( Q_{cb} \). With a sufficiently large gain in the push-pull inverter-type feedback amplifier, the total transconductance of the element is approximately equal to the linear input conductance \( 1/R_{in} \), thus linearizing the voltage-to-current conversion. The local negative feedback also increases output impedance of the transconductor. The input resistance \( R_{in} \) and capacitance \( C_{in} \) of the cell are chosen to be external for measurement purposes.

The four integration clock phases of the charge-domain sampler are generated from an external 200 MHz clock signal using synchronous logic with high-speed true-single-phase clocking (TSPC) flip-flops [9]. The external clock signal is further divided asynchronously by four to provide a clock signal for the standard CMOS logic controlling the pMOS switch matrices of the complex IIR filter.

IV. MEASUREMENT RESULTS

In measurement setup, the single-ended IF input signal of the circuit and the 200 MHz clock signal were obtained from external signal generators. The pseudodifferential outputs of the quadrature channels were sampled with two separate 14-bit fully differential A/D converters clocked with a synchronization signal from the test chip. A logic analyzer was used to transfer the output data to a PC for further processing.

Fig. 8 presents the measured and ideal gain-normalized complex amplitude responses of the sampler for positive and negative input frequencies from \( f_c - 3 f_s / 2 \approx 48.44 \) MHz to \( f_c + 3 f_s / 2 \approx 51.56 \) MHz. It can be seen that the simultaneous control of sampler’s both filtering functions by the same clock signals and sampling capacitances produces an accurate combined amplitude response for positive input frequencies. The measured 3-dB bandwidth of the complex IIR filter is 26.3 kHz around the 49.985-MHz IF input, corresponding to a low IF of \(-14.5 \) kHz. The suppression of the nearest unwanted frequencies aliasing on top of the wanted signal at the low IF, i.e., the built-in anti-aliasing suppression, is more than 34 dB. The measured attenuation for the first notches of the sampler’s FIR response at \( f_c \pm f_s \) is near 60 dB. The response for negative input frequencies, and hence the IMR, is degraded due to amplitude and phase mismatches in the I and Q signal paths and due to static timing errors in the integration clock phases. The measured IMR is over 44 dB on the whole 3 dB bandwidth of the circuit.

Worth noticing is that the parallel path mismatches can also cause spurious tones to appear at the output of the sampler. However, the use of relatively large capacitors in the circuit alleviates markedly all effects of path mismatches. The level of the strongest spurs for the test chip due to path mismatches was measured to be c.a. \(-64 \) dBc for a 0 dBV output signal at the passband. Note also that transferring the sampler’s output signal as a charge to a subsequent discrete-time signal processing stage allows minimizing spurs due to mismatches in absolute capacitor values, since thereby the capacitors are merely used as charge storage elements in the sampler stage.

The linearity of the circuit was measured by using a two-tone test. The input tone frequencies, separated by 1.5 kHz, were chosen so that both the resulting output signal tones and their third-order intermodulation (IM3) products lay within the passband of the complex IIR filter. The measured I channel output signal and IM3 levels as a function of input amplitude for nominal voltage gain (\( G_m \approx 0.1 \) mS, \( R_{in} = 10 \) k\Omega) are shown in Fig. 9. The measured extrapolated third-order input intercept point (\( \text{III}_3 \)) equals to \(-8 \) dBV. For high in-band input signal levels the output signal distortion results mainly from the sampler’s back-end active integrator stages, whose opamps have a limited output swing to handle the relatively high voltage gain of the sampler. Note that in the used \( G_m \) topology \( \text{III}_3 \) can be increased simply by increasing the input resistance.

The output noise of the test chip was integrated on the 26.3-kHz 3-dB bandwidth of the complex IIR filter to evaluate the spurious-free dynamic range (SFDR) of the circuit. The noise floor measured from the I channel output equals to
\[ 1.16 \text{ mV}_{\text{rms}} = -58.7 \text{ dBV}_{\text{rms}} \]
at the nominal gain. The SFDR was calculated from a two-tone test as amplitude difference of one output signal tone and the corresponding IM3 component at the output noise level. Both the input tones and their IM3’s
were selected to be on the passband of the IIR filter. The SFDR was measured for different voltage gain configurations of the circuit by altering the input resistance of the $G_m$ cell, which determines its transconductance gain ($G_m \approx 1/R_{in}$). The measured SFDR as a function of $R_{in}$ is presented in Fig. 10.

The measured SFDR at the nominal gain ($R_{in} = 10$ kΩ) is 59 dB. Fig. 10 indicates that the SFDR is little changed for $R_{in}$ values larger than 3 kΩ. Thus, automatic gain control (AGC) operation could be integrated into the realized sampler topology without significantly changing its dynamic range performance by altering the value of $R_{in}$, as long as certain minimum value for it is assured. As the voltage gain of the sampler is almost linearly inversely proportional to the input resistance, altering $R_{in}$, e.g., on the range 100 Ω–10 kΩ would provide 40 dB of AGC.

The measured main performance parameters of the test circuit are summarized in Table I. The chip microphotograph is shown in Fig. 11.

### Table I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input IF frequency</td>
<td>44.985 MHz</td>
</tr>
<tr>
<td>Output sampling frequency</td>
<td>1.042 MHz</td>
</tr>
<tr>
<td>Low-IF frequency</td>
<td>14.5 kHz</td>
</tr>
<tr>
<td>3-dB bandwidth</td>
<td>26.3 kHz</td>
</tr>
<tr>
<td>In-band IIP3</td>
<td>-8 dBV</td>
</tr>
<tr>
<td>IMR</td>
<td>60 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>44 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>85 mW @ 5 V</td>
</tr>
</tbody>
</table>

A circuit technique is presented for combining both complex FIR and IIR filtering functions into high-frequency bandpass signal sampling. The FIR filtering operation is achieved in the sampler by multiple weighted accumulation of integrated input current samples. The complex FIR response provides internal image rejection and anti-aliasing suppression prior to quadrature downconversion to a lower frequency by subsampling. The single-pole complex IIR filtering function takes place at the output subsampling rate of the sampler and increases selectivity of the circuit alleviating the linearity requirements for subsequent channel selection filter stages in a radio receiver chain.

The measured results of an example circuit-level FIR/IIR IF-sampler realization demonstrate the feasibility of the technique and show an accurate filtering response controlled by the sampling clock frequency and capacitance ratios, as well as high image band rejection without any tuning or trimming. Although an active integrator-based sampler realization is presented in the paper, a passive integrator-based implementation of the structure is also possible to minimize power consumption.

### REFERENCES


Sami Karvonen received the M.Sc.Eng. degree (with honors) in electrical engineering from University of Oulu, Oulu, Finland, in 2001. Since 2001, he has been working toward the Dr.Tech. degree at the Electronics Laboratory, Department of Electrical and Information Engineering, University of Oulu. His research interests include high-speed charge-domain sampling circuits and their applications to radio receivers.

Thomas A. D. Riley (M’82) received the B.E.Sc. degree from the University of Western Ontario, London, ON, Canada, in 1982, and the M.Eng. degree from Carleton University, Ottawa, ON, Canada, through a co-operative research program with Mitel Semiconductor in 1989. From 1982 to 1986, he was with Phillips Cables, Brockville, ON, a high voltage cable manufacturing company. Since 1995, he has been a Researcher at the University of Oulu, Oulu, Finland. He has also worked with Philsar Semiconductor, where he developed three fractional-N synthesizer chips.

Sami Kurtti was born in Kuusamo, Finland, in 1979. He received the M.Sc.Eng. degree (with honors) in electrical and information engineering from the University of Oulu, Oulu, Finland, in 2004. Since 2004, he has been working toward the Dr.Tech. degree at the same university. His research interests include the development of pulsed time-of-flight laser ranging techniques.

Juha Kostamovaara (M’85) received the Dipl.Eng., Lic.Tech., and Dr.Tech. degrees in electrical engineering in 1980, 1982, and 1987, respectively. He was Acting Associate Professor of electronics at the Department of Electrical and Information Engineering, University of Oulu, Finland, from 1987 to 1993 and was nominated Associate Professor in 1993. In 1994, he was an Alexander von Humboldt Scholar at the Technical University of Darmstadt, Germany. In 1995, he was invited to become a full Professor of electronics at the University of Oulu, where he is currently also head of the electronics laboratory. His main research interests include the development of time-to-digital converters, timing pick-off circuits, optical transceivers and frequency synthesizers for optical measurements and telecommunications. His group also develops pulsed time-of-flight laser radar techniques especially for industrial applications.