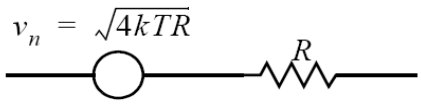
ELEC 4505 Changes from 2006 to 2007 (note page numbers refer to 2006 notes, 2007 page numbers are generally 1 page higher because old notes had page 1 then page 1a, new notes called this page 2.). 2004 Notes are very similar to 2006 notes, except as noted.
Outline: Added statement about accommodation

p. 5 Old notes said "Fortunately, a filter with 200 MHz cutoff at 900 MHz is not too difficult" this was changed to "Fortunately a filter which removes components more than 200 MHz from the carrier is quite achievable although still not easy"

p. 7 Bottom of page, add to noise section, "In class: show small-signal transistor model with noise, g_m, r_π, r_e, principle of design." (Bottom of 2007 page 7 shown here)

Resistor Model

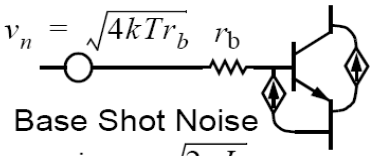


at $T = 297\,\text{K}$, $kT \approx 4.15 \times 10^{-21}$ W/Hz

at $R = 50\Omega$, $4kTR \approx 8 \times 10^{-19}$ V²/Hz

and $\sqrt{4kTR} \approx 0.9$ nV/$\sqrt{\text{Hz}}$

Transistor Model



where I_B and I_C are base and collector bias currents and q is the charge on an electron, $q \approx 1.6 \times 10^{-19}$

in class: show small-signal transistor model with noise, g_m, r_π, r_e, principles of design.

---

p. 8 in noise discussion, add the equation $F = \dfrac{N_{o,Tot}}{N_{o,Src}}$

p. 8 at bottom of page equation for cascaded noise add (simplify in class)

p. 14 Gain Estimate, first equation load is $R_C \| R_L$

p. 15 middle of page, as on previous page, load is $R_C \| R_L$

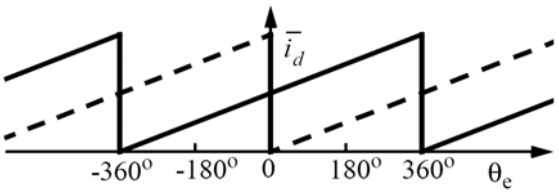
p. 15 towards bottom "At w and L resonate resulting in peak gain of" is replaced by "At resonance, the term in the bracket disappears and peak gain is"

p. 29 bottom of the page, retyped the bottom paragraph as the original was lost. However, the old version is correct while the 2007 version has a few typos, including "do to" instead of "due to", and other minor differences in wording, e.g., capacitance instead of capacitor.

p. 42 just after Principles of Operation, $kT/q = v_T$ (instead of v_t).

p. 65 The figure has x axis numbers not correctly positioned for 2, 3, 4, and 5 (2 is shown at 1.5, 3 at 2, etc)

p. 70 Figure had arrows removed and secondary plots were made dashed as shown at right.



p. 80 Last line of VCO paragraph changed to: "In these notes, frequency synthesizers using phase-locked loops are discussed in the section on phase-locked loops."

p. 80 end of Discrete vs Integrated Inductors – removed the fragment "At 2 GHz"

Two extra pages not in the 2004 notes are shown on the next two pages.

Extra Section: Mostly Page 2 in 2007 notes, Page 1b in 2006 note, missing from 2004 notes.

Higher Level (covered in other courses)

At the higher level, there are a lot of details we will not get into in this course. For example, there is signaling, call setup and control, identification, billing, testing, tracking, coding and error correction, that goes on in many communications systems for example, in a landline phone, or a cellular phone. Some of this is handled by DSP in the backend of the communications transceiver, but a lot of it is done by, or controlled by, the central office for landlines or the base station in cellular communications.

As an example, when a landline phone is picked up, the user hears a dial tone, the number is entered, the user hears the phone ring, and the other party picks up the phone and says "Oui hello?". This seems straightforward, but actually involves a complex set of signals and behind-the-scene actions, some of which will now be briefly described.

Taking the phone "off hook" closes a switch that starts current flowing. The central office detects that the phone is off hook, and connects a dial tone generator to the phone, so the user hears a dial tone, indicating the system is ready.

Entering a number on a touch tone system sends a number of tones back to the central office. These tones are converted back into numbers which are used to route the call, starting with country code, area code, then to the particular central office which is connected to the destination phone. Communication between central offices is generally all digital and at much higher data rates, so there is a whole host of conversions that take place as the signal is digitized and interleaved (multiplexed) with other messages being sent, converted to higher frequencies, possibly converted to be sent over different media (for example, fiber, microwave link, etc).

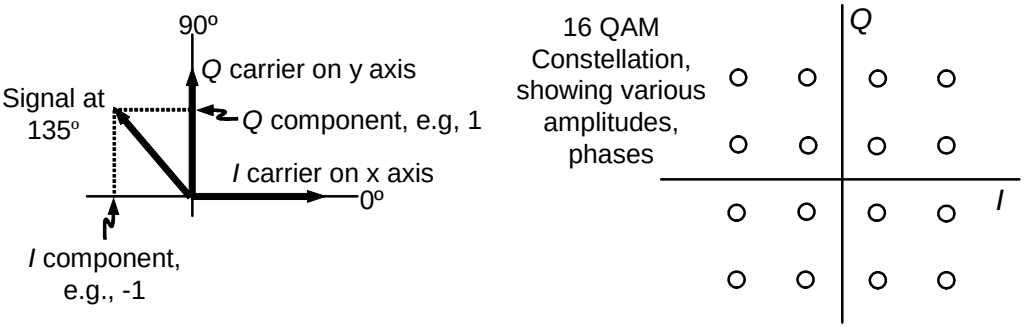
In any case, with very little delay, the central office on the far side (or the base station if the destination is a cell phone) checks the status of the phone on the far side. If it is available, it sends a ringing signal. At the same time, a ringing signal is sent back to the phone on the near side so the original person knows the phone on the far side is being called. If the far-side phone is being used, a busy signal is sent back to the first phone.

When the far side phone is picked up in response to the ringing, the far-side central office detects the off-hook condition and stops sending a ringing signal. Instead the "Oui Hello?" voice signal in the central office is digitized, coding and signalling information is added and the bits are interleaved (multiplexed) along with potentially multiple other conversations and sent along high speed links back to their various destinations. At the near side, all conversations intended for the near side are decoded, demultiplexed, and turned back into an analog electrical signal and connected to the correct line so the originating person hears the response. At the same time, the central office starts timing the call for billing information. And all of this takes a few tenths of a second.

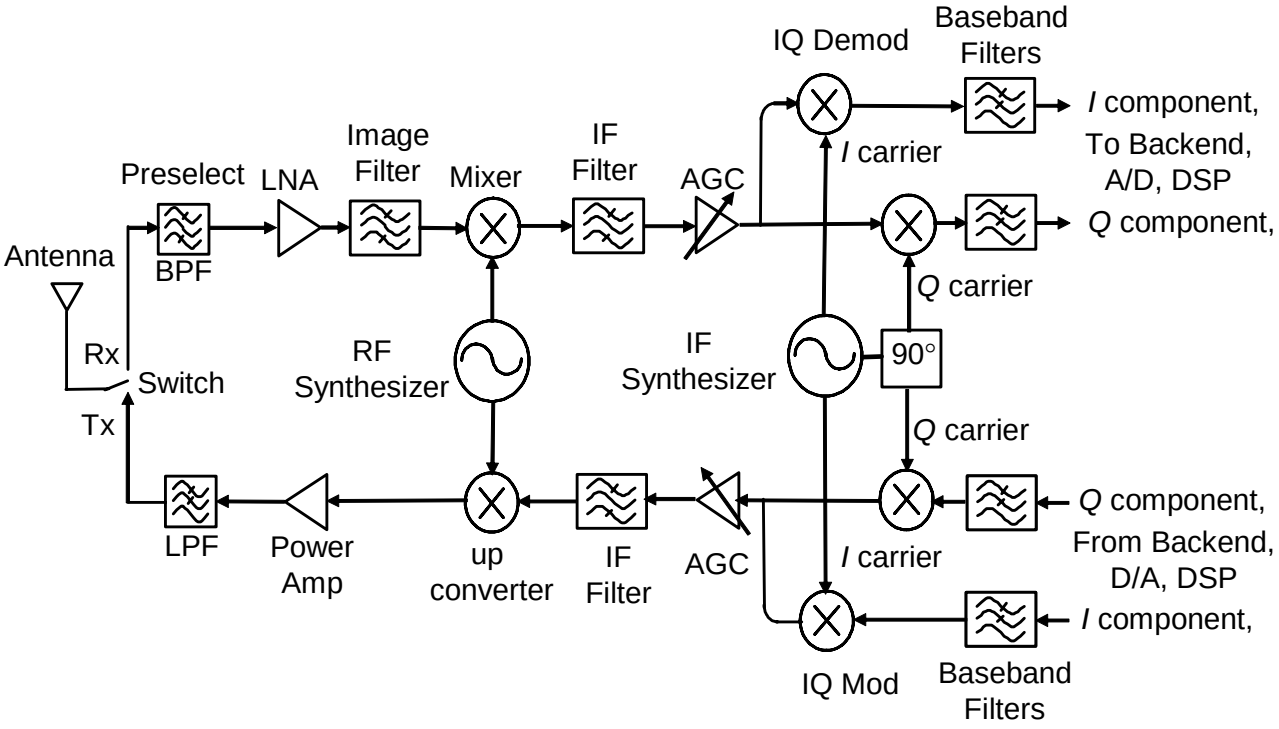
Note that in a plain landline phone, conversions between the analog voice signal and digital words usually takes place in the central office, while in the modern cell phone such conversions are done in the cell phone. The digital bits are used to modulate the cell phone carrier frequency. In a cell phone, there may be further signalling, for example, once call set-up is complete, a particular channel will be assigned, to allow multiple cell phones in the same area to be in use simultaneously yet independently. Other interventions by the base station is for hand-offs as a user crosses cell boundaries, or there may be the need for power control to keep the signal levels constant as the user moves with respect to the base station. In any case, it should be apparent that there is a lot that goes on in communications systems besides simply designing amplifiers, mixers, oscillators, etc.

I, *Q*, Modulation, Demodulation, Amplitude, Phase, etc.

We start with two carriers, one at 0° called the *In Phase*, or *I* component, the other at 90° called the *Quadrature Phase*, or *Q* component. By amplitude modulating these two carriers, then adding the result before transmitting, any phase can be created. For example, if *I* is 1 and *Q* is 1, we have 45°. if *I* is -1 and *Q* is 1, we have 135° as shown below. To detect a phase, we split the incoming signal into two paths, and mix one with an *I* carrier and the other with a *Q* carrier and the resulting two IF signals represent the *I* and *Q* modulation from which phase information can be extracted. Obviously, by changing the relative amplitudes of the *I* and the *Q* components, we can change the phase. And, since phase can change as a function of time, *I*, *Q* mod or demod can also be used for FM signals. It is also clear that amplitude can be changed thus this is a general technique for phase, amplitude and frequency modulation or demodulation. An example modulation scheme that uses both AM and PM is QAM, with a constellation for 16QAM below right. Thus, *I* and *Q* signals will each be four levels, together defining the 16 possible amplitudes and phases.



Below we see a full transceiver with *I*, *Q* paths to both the transmit and the receive side. In this diagram, splitting into *I*, and *Q* paths is done after the IF stage.



Lab differences:

Lab 1 2007 (P. 114 2006) Operation at 9 MHz, BW = 1.5 MHz, change throughout the lab. For frequency Multiplier, since centre frequency is 9 MHz, inputs are at 4.5 MHz, 3 MHz and 2.25 MHz, for the output to be at 9 MHz. For design, use inductors between 0.2 and 1 μH, $Q = 50$.

Lab 2 2007 (p. 124 2006) Carrier at 900 kHz, 100 mV rms, Modulating signal at 45 kHz, 200 mV rms. Since the step by step instructions have changed a bit for 2007, (at least compared to the 2004 notes) the full set of instructions has been shown below. Note, the figures are the same, so are not shown.

p. 125 2007 notes have new data sheets for the mixer on pages 129-138 which are a bit easier to read than the previous photocopies of photocopies. An added bonus is that this is for the dual inline package only, so pin numbers are correct on all diagrams. In 2006, there was a warning about incorrect pin numbers, which is correct for 2006 data sheets, but no longer needed for 2007, hence removed from the 2007 notes.

Lab 2 Mixer Design Instructions as in 2007 Lab Book. A number of small differences, so they have all been listed here.

1) Observe the output on an oscilloscope without the modulating signal input. What happens when the carrier null is adjusted? What is the frequency of the output signal at the null? (The signal should be small, but you should still be able to estimate frequency.)
2) Adjust the carrier null for MINIMUM carrier output. This corresponds to a balanced mixer. Now apply a modulating signal input. For a carrier input level set to 100 mV RMS and the modulating signal set for 200 mV RMS measure the double sideband output signal amplitude. Compute the double sideband output signal amplitude for the above values and compare the results with the measured value.
   Several Notes:
   a) With a carrier frequency of 900 kHz and a modulating input at 45 kHz, there are 20 cycles of the carrier per cycle of the modulating waveform. If the DSBSC envelope is not apparent, you should make sure you are triggering on the modulating input signal. Use of a lower modulating frequency, for example 20 kHz, can also help to see the envelope.
   b) The gain table in the data sheets gives v_o/v_m for AC and DC at: i) low levels of the carrier where the amplitude of the carrier is important and ii) at *high carrier levels where its amplitude is no longer important since at large voltages it serves to switch the input transistors completely on or off. Your job is to determine if the operation is small or large signal and use the appropriate formula. Alternatively you could use the graphical approach by using Figure 11 of the data sheets.*
3) Using the spectrum analyzer built into the oscilloscope (math function), plot the output of the balanced modulator in the frequency domain. Vary the modulating signal frequency and note what happens. Note a double sideband signal on an oscilloscope in the time domain will look very much like an AM modulated signal with much sharper zero crossings. See Fig 1 and 3 on the data sheet.
4) For a fixed carrier and modulating signal frequency plot the magnitude of the voltage transfer function of the balanced mixer. The carrier level will be fixed at 100 mV RMS and the modulating signal level will be varied. Find the range over which the device is approximately linear. Compare this to the theoretical linear range given on page 8-19 and 8-20 of the data sheets in the “Signal Levels” section.

5) Design a tuned circuit for the sum of the carrier and modulating signal frequencies and place it on one of the outputs (see Fig3). This is to extract the upper sideband or the f1 + f2 component. (You will have some inductors available to build a tank circuit, more details will be provided later). Remember to remove the 3.3kΩ resistor. Note the output waveform. If the centre frequency of your tuned circuit is off a bit, don't readjust, just move your carrier frequency until the sideband falls in the filter passband. Verify that all frequencies are correct and as expected.
6) Compute the amplitude of the output signal. Note that at resonance, the load resistance is the parallel combination of the load resistor, the output resistance of the modulator (given in the data sheets) and the equivalent inductor parallel resistance.
7) Observe and sketch the output in both the time domain and frequency domain, and compare the amplitude to the calculated amplitude.
8) Retune the tuned circuit (or adjust the centre frequency) so the difference frequency, (the lower sideband) falls into the filter passband. Verify all frequencies are correct and as expected.
9) Again, observe and sketch the output in both the time domain and frequency domain, and compare the amplitude to the calculated amplitude.

Lab 3 2007 (p. 138, 2006) Target Frequency is 900 kHz. In the frequency synthesizer part, the reference frequency is nominally at 225 kHz, so with a divide by 4 in the feedback, the output is at 900 kHz. With a divide by 3 in the feedback, the output will be at 675 kHz.

Step 13 reference is made to ω_n of 2000 Hz, in the old notes instead of ω_n, it said loop bandwidth. Step 20 it In the 2004 notes it mentions a ratio of 6:1 and 8:1, this should be 3:1 and 4:1.

At the end, added reference [7] Rogers, Plett, Dai, *Integrated circuit Design for High Speed Frequency Synthesis*

End of Course Notes:

p. 151 and on – for 2007 added the 2006 exam, removed 2001, 2000 exams, added answers for 2006 exam, removed answers for 2001, 2000 exams.

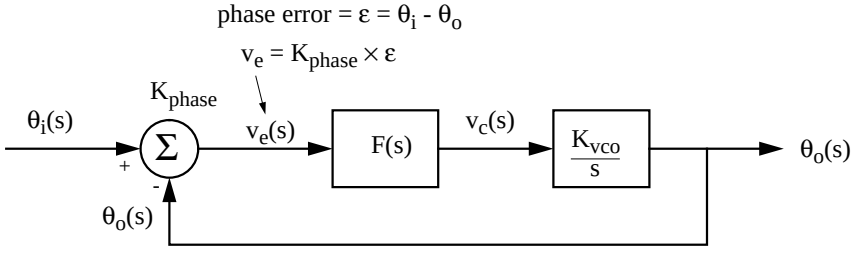
p. 177 solution to Q3c of 2002 exam, capacitor should be 138.9 pF.

p. 181-187 removed these extra pages from the 2007 notes as these are not providing much (if any) additional useful information.

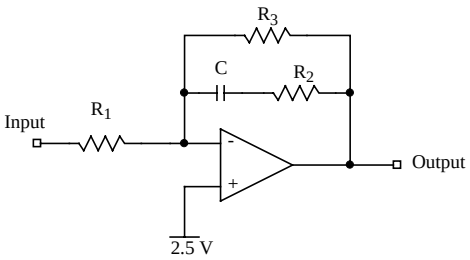
Assignments 2 and 3 have been added on the next three pages, exactly as they appear in the 2007 course notes.

Note that the first three questions are closely related to Lab 3. Be sure you save your calculations for the lab (remember you hand in the assignment just before you do the second half of the lab).

1. Solve for the loop filter transfer function F(s), and use it to find the PLL transfer function (θ_o/θ_i) and the phase error transfer function (ϵ/θ_i) (in terms of R and C, etc, not F(s)). Do not use any simplifying approximations for the loop filter until Question 3.



PLL



Loop Filter

2. Now using the equations derived above, determine the values for the loop filter components such that the natural frequency of the feedback system is 2000 Hz and the damping coefficient is 1.0. Use a loop gain equal to $2 \times K_{phase}K_{vco}$. This means that your loop filter should have a gain of 2 at DC. You will need to use your measured value for K_{vco} (it might be approximately $K_{vco} = 2\pi \times 5 \times 10^5 \pm 50\%$ (rad/sec)/V). If you are using phase detector I, use $K_{phase} = 1.6$ V/rad. For phase detector II use $K_{phase} = 0.4$ V/rad.

3. For the above filter, determine under what conditions (components, frequencies) the simpler expressions as derived in class for the integrator and phase lead correction may be used. Does this apply to your component values?

4. Specify ω_n and ζ for a loop that will settle from a 40 kHz input frequency step in about 50 μs (or less), with a maximum phase error during the transient of about 45° ($\pi/4$ radians) (or less). The phase detector is an exclusive-or gate and the loop filter is an integrator with phase-lead correction. Sketch the approximate phase error versus time. Also, calculate the minimum frequency step which would cause the loop to lose lock during the transient.

5. We have a second-order loop with an integrator with phase-lead correction. The input signal to the loop f_i is a 1 MHz frequency modulated signal with a frequency deviation Δf of 300 Hz. As the modulating frequency f_m is changed we note that the maximum phase error ϵ_p is 0.6 rad and occurs for a modulating frequency $f_m = 250$ Hz. What is the damping constant ζ and natural frequency ω_n of the loop?

   Note that for input modulating frequencies less than 250 Hz, the phase error is less than 0.6 rad. Now for the same Δf, ω_n, and ζ as above, determine the input modulating frequency range (lower than 250 Hz) for which the phase error would be less than 0.3 radians.

6. A PLL synthesizer is required which generates frequencies from 49 MHz to 51 MHz in 500 kHz steps. Draw a block diagram of the synthesizer, label each part and determine what frequencies and (integer) divider values are needed. Assume a reference at 1 MHz is available.

   If the 1 MHz reference now drifts in frequency by 1 kHz, (that is, its frequency changes by 1 kHz) what does this do to each of the 5 output frequencies?

Oscillator Design (Impedance matched to resistive load. Open-loop, closed-loop simulation.)

The following circuit is a Colpitts oscillator with the base grounded. Compared to the common-emitter version shown in the lectures, this allows higher frequency operation because Miller multiplication of C_{bc} has been eliminated. However, because of the presence of R_e and the equivalent emitter input resistance r_e, the analysis is more complicated. Instead, design will follow simple guidelines, followed by simulations.

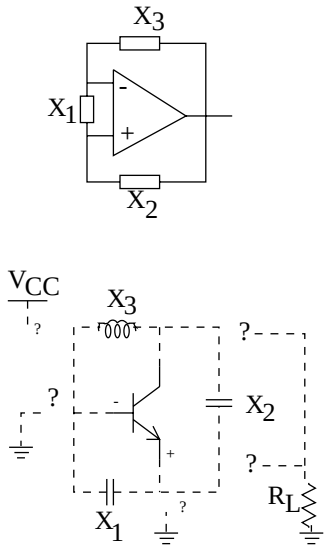


Fig 1 a) Oscillator with Amplifier b) with Bipolar Transistor

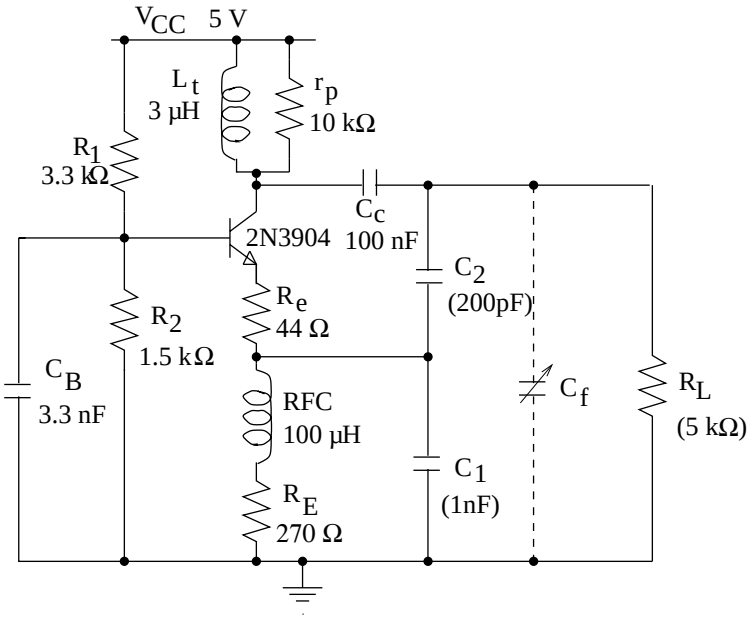


Fig 2 Colpitts Oscillator with Grounded Base.

1. Calculate your desired frequency of oscillation f_o as (9 + xx/49.5) MHz, where xx represents the last two digits of your student number. This will result in f_o between 9 and 11 MHz.
2. Find the required components by using the following design procedures and approximations.
   a. First, establish the operating point, i.e., V_C, V_B, V_E, I_C, g_m and r_e (collector, base, emitter voltages, transistor current, transconductance and equivalent emitter resistance). V_B is set by the voltage divider, R_1 and R_2. V_E is a diode drop below V_B. I_C is set by V_E and the resistive load, $R_e + R_E$. Determine $g_m = I_C/v_t$ where v_t, the thermal voltage, is approximately 25 mV at room temperature. Then, $r_e \approx 1/g_m$.
   b. Calculate the resistor value R_L so that it dissipates about 3 mW of power. Note that the peak-to-peak output voltage will be about the same as peak-to-peak voltage at the collector. The collector voltage is nominally at V_{CC} with a peak downward swing to about V_E.
   c. Then calculate the capacitor values by noting the conditions for oscillation and the best impedance match for the maximum power transfer to the load. Note that C_f could be used for frequency tuning, however for simplicity, it is to be left out in this assignment.

i. The frequency can still be estimated by $X_1 + X_2 + X_3 = 0$.

ii. In general, impedance match means conjugately matching the load to the complex driving impedance. At resonance, however, only a resistive match is required. Thus, R_L is matched to the driving resistance which is made up of r_p, in parallel with R_{eq}, the equivalent resistor seen due to $r_e + R_e$. It can be shown that R_{eq} is transformed from $r_e + R_e$ by the capacitive transformer formed by capacitors C_1 and C_2 with a "turns ratio" of approximately $\frac{C_1}{C_s}$ where C_s is the series equivalent capacitance of C_1 and C_2. This results in an increased equivalent resistance approximately equal to $R_{eq} = (r_e + R_e) \times \left(\frac{C_1}{C_s}\right)^2$. The required R_{eq} sets the ratio of C_1 and C_2 while the frequency of oscillation sets the series combination of C_1 and C_2 (or C_s). Thus both C_1 and C_2 can be found.

3. Perform an open-loop frequency-domain simulation and predict the frequency of oscillation and determine the gain margin. Open the loop at the emitter making sure to load the other end by $r_e + R_e$ as shown in Figure 3. The frequency of oscillation is given by the frequency at which the phase is 0°. The gain at this frequency, known as gain margin tells us how much the gain could be reduced before the oscillator would no longer oscillate.

4. Then, close the loop (Figure 2) and simulate in the time domain to observe the oscillations. To start the oscillations, feed a pulse of current into the collector with a current of about $I_{DC}/5$ a pulse width of about T/3 and a rise and fall time of about T/10 where T is the expected period of oscillation. This should be successful, but if not, you could increase the current or decrease the rise and fall times. Observe the startup transient, the oscillation amplitude and frequency and compare to the expected results.

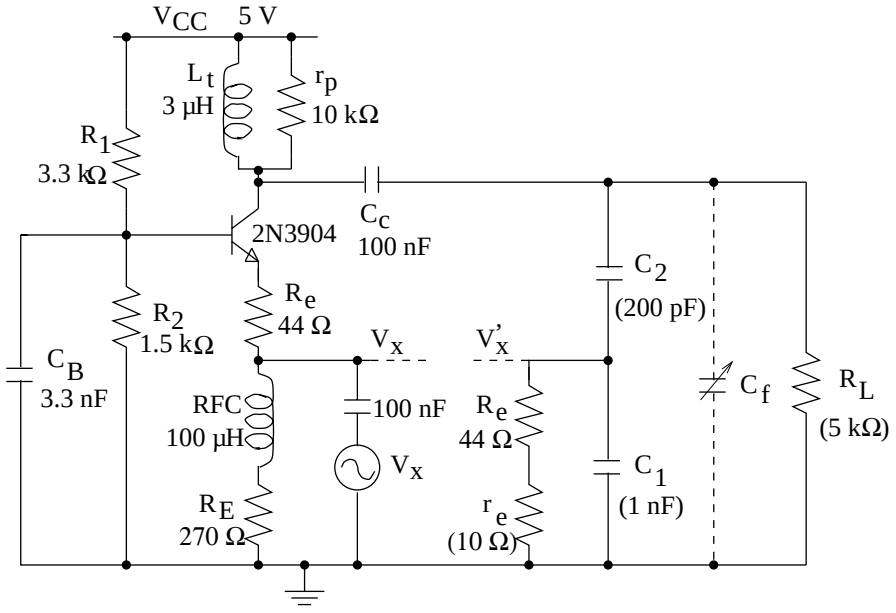


Fig 3 Open-Loop Colpitts Oscillator.

CARLETON UNIVERSITY

FINAL
EXAMINATION
December 2006

DURATION 3 **HOURS** No. of Students 53

Department Name & Course Number: Electronics ELEC 4505
Course Instructor(s): Prof. Calvin Plett

AUTHORIZED MEMORANDA: Calculators Allowed

Students MUST count the number of pages in this examination question paper before beginning to write, and report any discrepancy immediately to a proctor. This question paper has 5 **pages.**

This examination question paper MAY **be taken from the examination room.**

Marks total to 84

Question 1 Transceiver and General Questions (Total 16 Marks)

A receiver has input frequencies from 902 to 928 MHz with a channel bandwidth and channel spacing of 1 MHz. Assume the desired channel is at 915 MHz and the IF is at 100 MHz.

5 marks (a) Sketch a block diagram of the above receiver from antenna to IF showing frequencies at each stage and approximate bandwidths of the filter(s). If two possible LO frequencies are found, use the higher one.

3 marks (b) What is the image frequency when the input is at 915 MHz? Where does the image signal come from and which circuit element deals with it?

4 marks (c) For an amplifier with gain of 20 dB and a noise figure of 3 dB, if the input signal is 10^{-12} W and the input noise power is $kTB = 4 \times 10^{-15}$ W from the 50Ω antenna input in a 1 MHz bandwidth, determine the output signal in W, and the output signal-to-noise ratio in dB.

4 marks (d) An amplifier has a transfer function of $v_o = 10(v_i - v_i^3)$. At the input, the desired signal at 915 MHz is 1 mV and two adjacent signals at 916 MHz and 917 MHz are each 100 mV. What will be the desired and undesired output signals at 915 MHz? What type of distortion does this problem illustrate?

Question 2 Tuned Amplifier (Total 17 Marks)

An amplifier has an input impedance at 1 GHz of $z_{in} = 80 - j400\ \Omega$.

2 marks (a) Determine y_{in}.

2 marks (b) Show the parallel and series equivalent input circuits valid at 1 GHz. Identify which of the two circuits corresponds more directly to z_{in} and which corresponds more directly to y_{in}.

6 marks (c) Design a transformer-based parallel input matching circuit to match a 50Ω source to the amplifier input, and to provide a 100 MHz bandwidth. Use a transformer with primary connected to the source and with secondary connected to the amplifier. Assume the secondary has an ideal inductance L and the primary inductance may be ignored. Show turns ratio, required inductance *L*, and any extra components required to achieve the required impedance match and bandwidth.

2 marks (d) If the inductor were not ideal, but had a quality factor of *Q*, describe how this would change the design in (c).

5 marks (d) Now remove the transformer-based matching circuit and instead design an LC input matching circuit to achieve match at 1 GHz between the 50Ω source and the amplifier.

Question 3 Class C Frequency Doubler (Total 9 Marks)

The transistor in a class C frequency doubler (a frequency multiplier with n=2) repeatedly conducts for 33.3 μs then is off for 66.7 μs. The peak transistor current is 100 mA and the power supply is 10 V.

2 marks (a) Determine the input frequency and the desired output frequency.

3 marks (b) Find the average power supply current.

2 marks (c) Find the output current at the desired output frequency.

2 marks (d) If the load resistor is 100Ω, determine the efficiency.

Question 4 Mixer (Total 12 Marks)

3 marks (a) A down conversion mixer as shown in Figure 1, used as part of a cell phone receiver has an input at the RF frequency and a local oscillator input. Describe why one of these inputs would need to be linear while the other one need not be. In the mixer as used in Lab 2, what technique was used to improve linearity of one of the mixer inputs?

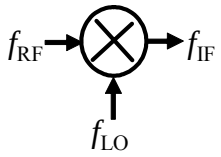


Figure 1

5 marks (b) Figure 2 shows the output waveform from an ideal up-conversion switching mixer. Determine the input modulating frequency and the carrier (switching) frequency. Sketch the frequency spectrum showing the amplitudes and frequencies.

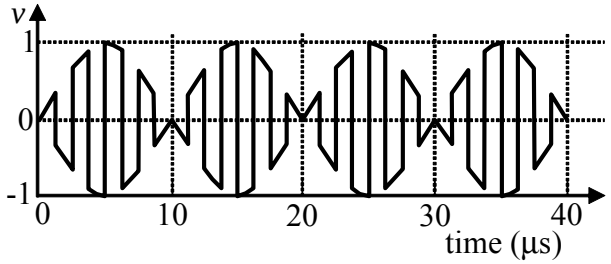


Figure 2

4 marks (c) The waveform of (b) is now connected to a bandpass filter which is designed to pass the upper sideband and attenuate the lower sideband by 20 dB. In the frequency domain, sketch the required filter response and the filter output spectrum showing the signal amplitudes. Also, sketch the resulting waveform in the time domain.

Question 5 FM (Total 4 Marks)

4 marks A 100 MHz carrier with an amplitude of 1V peak is frequency modulated with a resulting frequency deviation of 10 kHz. The modulating signal is at 25 kHz. Sketch the approximate output frequency spectrum clearly showing amplitudes and frequencies.

Question 6 Phase-Locked Loop (Total 17 Marks)

Figure 3 shows the loop gain of a phase-locked loop with a K_{VCO} of 10^7 rad/s/V and an exclusive-nor-gate phase detector with K_{phase} of 1.6 V/rad. Assume there is no additional gain block in the loop, that is, assume $A_0 = 1$.

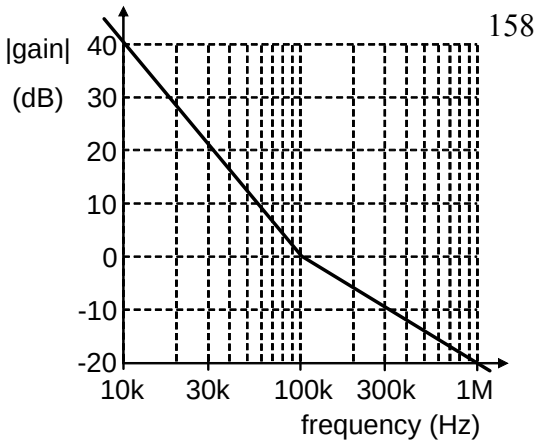


Figure 3

5 marks (a) What type of loop filter is being used? Determine its time constants and its transfer function.

4 marks (b) Determine the parameters of the closed-loop PLL including K, natural frequency ω_n, and damping constant ζ.

3 marks (c) Determine how large a frequency step the phase-locked loop would be able to track without losing lock. Estimate the approximate settling time for such a frequency step.

5 marks (d) Sketch the phase corresponding to the magnitude shown. Explain the stability or lack of stability.

Question 7 Oscillator (Total 9 Marks)

Figure 4 shows a Colpitts oscillator with a common-emitter amplifier. Assume the transistor has a low frequency β of 100 and an f_T of 1 GHz.

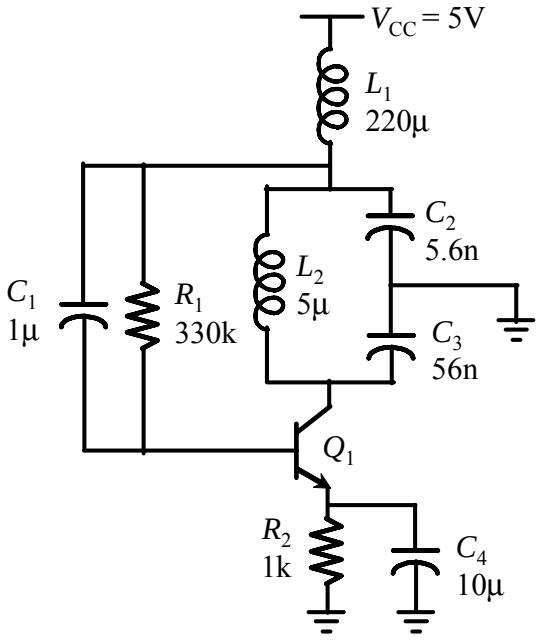


Figure 4

3 marks (a) Estimate the collector current and the voltages on the transistor terminals.

3 marks (a) Identify the main circuit elements which determine the oscillation frequency.

3 marks (b) Determine the oscillating frequency and the required gain. Is the gain condition met for this particular oscillator?

ELEC 4505 Formula Sheet 2006 revision 1

Noise Figure

$$\text{NF} = 10\log_{10}\frac{(S/N)_{in}}{(S/N)_{out}} = 10\log_{10}\frac{N_{out}}{GN_{in}}$$

Resistor Noise $= 4kTR$ in V^2/Hz where $KTR \approx 2\times10^{-19}\ V^2/\text{Hz}$ for R=50 Ω, $T = 297\ K$.

h-parameters

$$\begin{bmatrix} v_{be} \\ i_c \end{bmatrix} = \begin{bmatrix} h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix} \begin{bmatrix} i_b \\ v_{ce} \end{bmatrix}$$

Inductor

If $Q_L \gg 1$ then $Q_L = \dfrac{\omega_0 L}{r_s} = \dfrac{r_p}{\omega_0 L}$

Tuned Circuit

$$B = \frac{1}{RC}, \quad \omega_0 = \frac{1}{\sqrt{LC}}, \quad Q = \frac{\omega_0}{B}$$

Transformer

$$\frac{v_2}{v_1} = \frac{n_2}{n_1} = \frac{i_1}{i_2}, \quad Z_1 = \left(\frac{n_1}{n_2}\right)^2 Z_2$$

General Formulas

$$\sin(\alpha \pm \beta) = \sin\alpha\cos\beta \pm \cos\alpha\sin\beta$$
$$\cos(\alpha \pm \beta) = \cos\alpha\cos\beta \mp \sin\alpha\sin\beta$$
$$2\cos\alpha\cos\beta = \cos(\alpha-\beta) + \cos(\alpha+\beta)$$
$$2\sin\alpha\sin\beta = \cos(\alpha-\beta) - \cos(\alpha+\beta)$$
$$2\sin\alpha\cos\beta = \sin(\alpha-\beta) + \sin(\alpha+\beta)$$

PLL Lock range $= \pm K = \pm K_{phase}K_{vco}A_0$ for sinusoidal phase detector, $\pm\frac{\pi}{2}K$ for X-Nor.

$$\frac{\theta_o}{\theta_i} = \frac{KF(s)}{s+KF(s)} \quad \frac{v_c}{\theta_i} = \frac{sK_{phase}A_0F(s)}{s+KF(s)}$$

$$\frac{\epsilon}{\theta_i} = \frac{s}{s+KF(s)} \quad \text{if} \quad F(s) = \frac{s\tau_2+1}{s\tau_1}$$

$$\text{then} \quad \frac{\theta_o}{\theta_i} = \frac{K(s\tau_2+1)}{\tau_1(s^2+2\zeta\omega_n s+\omega_n^2)}$$

$$\text{where } \omega_n = \sqrt{\frac{K}{\tau_1}} \text{ and } \zeta = \frac{\omega_n\tau_2}{2}$$

Mod. Bandwidth Estimate $W < 2\omega_n\zeta$

FM input : max phase error at $\omega_m = \omega_n$, $\epsilon_p = \left(\dfrac{\Delta\omega}{\omega_n}\right)\dfrac{1}{2\zeta}$

Distortion and Linearity inputs at f_1, f_2, intermod IM3 at $2f_1 - f_2$ and $2f_2 - f_1$. $P_o \propto P_{in}$, IM3 $\propto P_{in}^3$. Intercept point: IP3 where P_o and IM3 have the same power.

Harmonics: HD2 at $2f_{in}$, HD3 at $3f_{in}$.

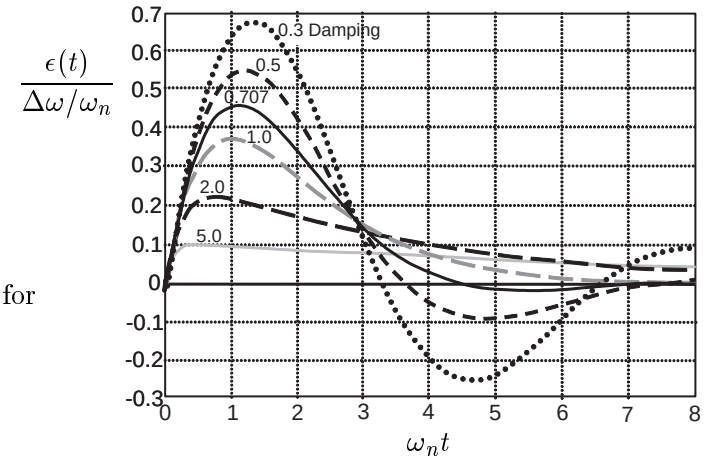
Class C and Frequency Multiplier

$$i_c = I_p(\cos\omega t - \cos\theta)$$
$$I_{DC} = \frac{I_p}{\pi}(\sin\theta - \theta\cos\theta)$$
$$I_1 = \frac{I_p}{2\pi}[2\theta - \sin 2\theta]$$
$$I_n = \frac{2I_p}{\pi}\left[\frac{(\cos\theta\sin n\theta - n\sin\theta\cos n\theta}{n(n^2-1)}\right]$$

(FM) for small $\beta = \frac{\Delta\omega}{\omega_m}$, $\gamma = \omega_c t$, $\alpha = \omega_m t$

$$\cos(\gamma + \beta\sin\alpha) \approx \cos\gamma - \beta\sin\alpha\sin\gamma$$

(AM) $A(1 + K\cos\omega_m t)\cos\omega_c t$



Bipolar Transistors

$$\beta = \frac{i_c}{i_b} \qquad g_m r_\pi = \beta \qquad g_m = \frac{I_C}{v_T}$$

$$\alpha = \frac{i_c}{i_e} = \frac{\beta}{\beta+1} = g_m r_e \qquad r_e = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$$

$v_T = 25$ mV at room temperature.

Oscillator

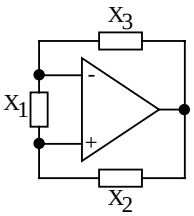
$$X_1 + X_2 + X_3 = 0$$

$$A_v \geq \frac{X_2}{X_1}$$

for amplifier with no input current, e.g., MOS where $A_v = g_m r_o$.

$$\beta \geq \frac{X_1}{X_2}$$

for amplifier with input current and current gain β, e.g., Bipolar



CARLETON UNIVERSITY

FINAL
EXAMINATION
December 2005

DURATION 3 **HOURS** No. of Students 60

Department Name & Course Number: Electronics ELEC 4505
Course Instructor(s): Prof. Calvin Plett

AUTHORIZED MEMORANDA: Calculators Allowed

Students MUST count the number of pages in this examination question paper before beginning to write, and report any discrepancy immediately to a proctor. This question paper has 5 **pages.**

This examination question paper MAY **be taken from the examination room.**

Marks total to 85

Additional formulas, probably not needed, are: $\beta=I_C/I_B$, $g_m r_\pi = \beta$, $g_m = Ic/v_T$, $\alpha = I_C/I_E = \beta/(\beta+1)$, $v_T \approx 25$mV at room temperature.

Question 1 Transceiver and General Questions (Total 16 Marks)

A receiver has input frequencies from 5.15 to 5.25 GHz with a channel bandwidth and channel spacing of 10 MHz (0.01 GHz). Assume the desired channel is at 5.20 GHz and the IF is at 300 MHz.

5 marks (a) Sketch a block diagram of the above receiver from antenna to IF showing frequencies at each stage and approximate bandwidths of the filter(s). If two possible LO frequencies are found, use the lower one.

3 marks (b) What is the image frequency when the input is at 5.20 GHz? Where does the image signal come from and which circuit element deals with it?

4 marks (c) In a narrowband receiver such as this one, which type of distortion is the most important one? Give an example of input frequencies for which such distortion could occur. How can such distortion be avoided?

4 marks (d) For an amplifier with gain of 20 dB and with bandwidth of 100 MHz, if the added noise power is three times as much as the noise power from the source, what is the noise figure of the amplifier?

Question 2 Tuned Amplifier (Total 18 Marks)

6 marks (a) Design a common-emitter amplifier (determine L_L, R_L, and C_L) as shown in Figure 1(b), with a tuned output load, a gain (v_c/v_b) of 20 dB, center frequency of 1 GHz and 3 dB bandwidth of 100 MHz. Assume the inductor has a Q of 50. The transistor model is shown in Figure 1(c).

3 marks (b) Now remove R_L and replace L_L with a transformer whose primary winding with N_1 turns, connected to the collector, has an inductance equal to L_L (with a Q of 50). The secondary winding, with N_2 turns (whose inductance may be ignored) is connected to a 50Ω load resistor. Determine the required transformer turns ratio N_2/N_1, and the voltage gain from the base to the load resistor.

4 marks (c) Find Z_{in} and Y_{in} of the amplifier, as indicated in Figure 1.

5 marks (d) Now design an LC input matching circuit to achieve match at 1 GHz.

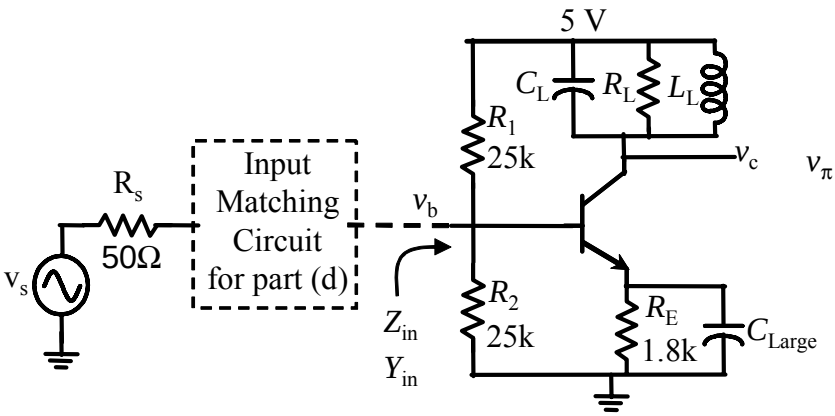
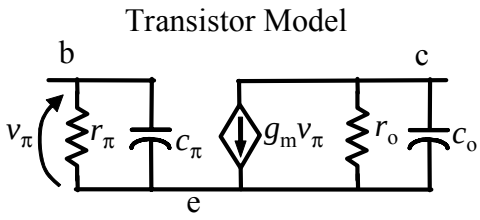


Figure 1(a)

Figure 1(b)



$r_\pi = 2$ kΩ $g_m = 50$ mA/V
$c_\pi = 0.4$ pF $r_o = 25$ kΩ
$c_o = 0.1$ pF

Figure 1(c)

Question 3 Class C Amplifier (Total 9 Marks)

The transistor in a class C amplifier conducts for 4 μs of every period where a period is 10 μs. The peak transistor current is 10 mA and the power supply is 10 V.

1 marks (a) What is the desired output frequency?

3 marks (b) Find the average power supply current.

2 marks (c) Find the output current at the desired output frequency..

3 marks (d) For what value of load resistor will the efficiency be approximately 50%?

Question 4 Mixer (Total 10 Marks)

5 marks (a) An ideal multiplier is used as a mixer. The two inputs are a 10 kHz signal at 1V peak and a 60 kHz signal at 2V peak. Show the output time-domain and frequency-domain waveforms and calculate the total output rms voltage.

5 marks (b) A bandpass filter with a center frequency of 70 kHz, as shown in Figure 2, is connected to the output. Sketch the output of the filter in the time-domain and frequency-domain.

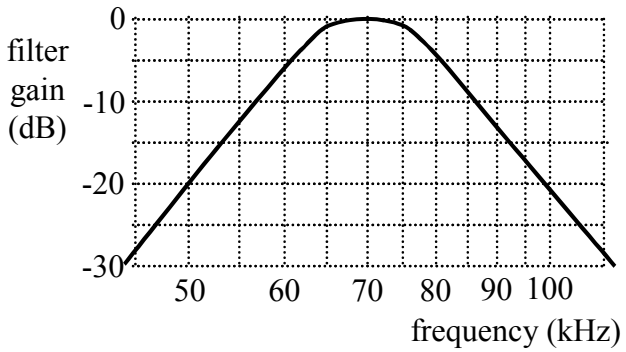


Figure 2

Question 5 Phase-Locked Loop with a Feedback Divider (Total 17 Marks)

A Frequency Shift Keying System switches frequency between 1.00 MHz and 1.01 MHz with a bit rate of 10 kbps (that is the frequency can change every 100 μ seconds. A PLL is required which will be able to follow this frequency step without losing lock and settle before the end of the bit period, that is, in less than 100 μ seconds. You have available a phase detector based on an exclusive-nor gate with $K_{phase} = 5/\pi$ (V/rad), and a VCO with $K_{VCO} = 1\times10^7$ rad/sec/V. You may use a loop filter with $F(s) = \dfrac{1+s\tau_2}{s\tau_1}$.

2 marks (a) What is the nominal phase and maximum phase error away from the nominal phase for an exclusive-nor gate phase detector?

3 marks (b) determine the center frequency, natural frequency, and damping constant such that the loop settles within the allowed time and does not lose lock.

3 marks (c) What is the maximum phase error during the transient? At what time does it occur relative to the frequency step? (If you discover maximum phase error is larger than specified in part (a) readjust loop parameters such that lock is not lost.)

3 marks (d) Estimate the loop bandwidth. Explain in a few sentences what is the significance of the loop bandwidth.

6 marks (e) Calculate the loop time constants. Sketch on a Bode plot the open loop gain and phase showing slopes, break point(s) and approximate unity gain frequency. Comment on stability.

Question 6 Oscillator (Total 9 Marks)

Figure 3 shows the start of a Colpitts oscillator with a common-base amplifier.

3 marks (a) Complete the oscillator showing the bias circuitry, power and ground. No component values are needed.

6 marks (b) Determine C_1 and C_2 values for an oscillating frequency of 1 GHz ensuring that the gain condition for oscillation has some margin (aim for a factor of 2). The transistor has an f_T of 10 GHz. Note, f_T is the frequency at which current gain is 1, and current gain is inversely proportional to frequency. Assume L is equal to 5 nH.

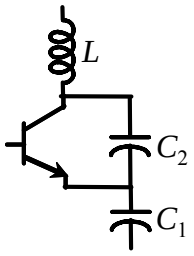


Figure 3

Question 7 Narrowband FM Waveform (Total 6 Marks)

6 marks (a) For the Narrow-Band FM waveform in Figure 4, find the equation describing the waveform. Determine the frequency components and the total rms voltage. Note, the waveform is not drawn to scale.

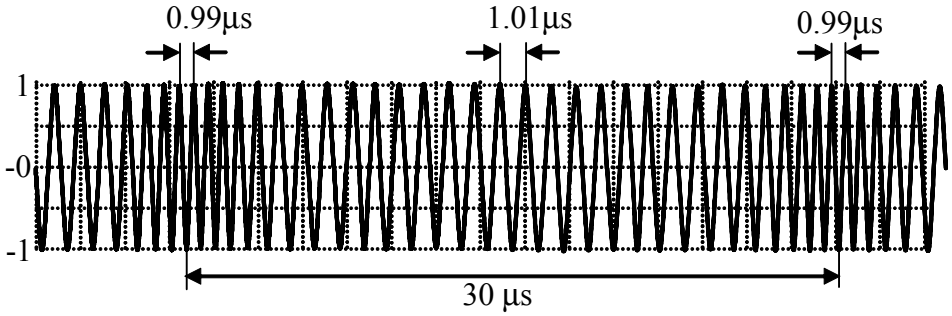


Figure 4

CARLETON UNIVERSITY

FINAL
EXAMINATION
December 2004

DURATION 3 HOURS No. of Students 73

Department Name & Course Number: Electronics ELEC 4505
Course Instructor(s): Prof. Calvin Plett

AUTHORIZED MEMORANDA: Calculators Allowed

Students MUST count the number of pages in this examination question paper before beginning to write, and report any discrepancy immediately to a proctor. This question paper has 5 pages.

This examination question paper MAY be taken from the examination room.

Marks total to 86

Additional possibly useful formulas are: $\beta=I_C/I_B$, $g_m r_\pi = \beta$, $gm = Ic/v_T$, $\alpha = I_C/I_E = \beta/(\beta+1)$, $v_T \approx 25$ mV at 27°C

Question 1 Transceiver and General Questions (Total 16 Marks)

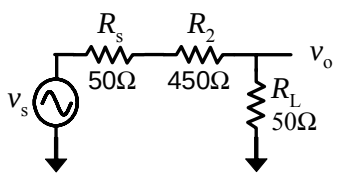
A transmitter has an input signal at 200 MHz. In the transmitter, this input is upconverted to one of a number of possible channels at RF. The local oscillator (LO) is designed to be tunable from 2.6 GHz to 2.7 GHz in steps of 1 MHz resulting in channel bandwidths of 1 MHz. Assume the nominal LO frequency is at 2.65 GHz.

5 marks (a) Sketch a block diagram of the above transmitter from the input 200 MHz signal to the antenna showing frequencies at each stage and approximate bandwidths of the filter(s). For any LO frequencies, if two possible output frequencies are found, use the lower one.

3 marks (b) What is the image frequency when the LO is at 2.65 GHz? Where does the image signal come from and which circuit element deals with it?

4 marks (c) Now consider a receiver. In a narrowband superheterodyne receiver, which converts input signals to an IF frequency, why is third-order intermodulation distortion more important than harmonic distortion? If the desired input frequency is at 2.45 GHz and channel spacing and bandwidth are both 1 MHz, give an example of the most likely input signals which could cause problems through this type of nonlinearity.

4 marks (d) A voltage divider (similar to the one which might be found in a passive probe) is added to an input source as shown at right. Calculate the noise figure. You may ignore noise originating from R_L.



Question 2 Tuned Amplifier (Total 20 Marks)

An antenna with an equivalent impedance of 50Ω is to be connected to a transistor amplifier through a tuned input matching circuit as shown in Figure 1. The transistor has a model as shown. For parts (a) through (d), the match will be done with a transformer with turns ratio of N_1 to N_2. The N_2 side has inductance L (with infinite Q). The N_1 side, connected to the antenna, has negligible inductance. The center frequency is 20 MHz and the bandwidth is 4 MHz.

3 marks (a) Find Z_{in} and Y_{in} of the amplifier, as indicated in Figure 1.

6 marks (b) Determine the value of L and any other components required to do parallel impedance matching.

2 marks (c) Determine the turns ratio N_2/N_1 for impedance matching.

3 marks (d) Determine the value of R_L in order to give an overall gain of 10 from v_s to v_o.

6 marks (e) Now replace the transformer-based input matching circuit with an LC matching circuit and calculate the component values to achieve match at 20 MHz.

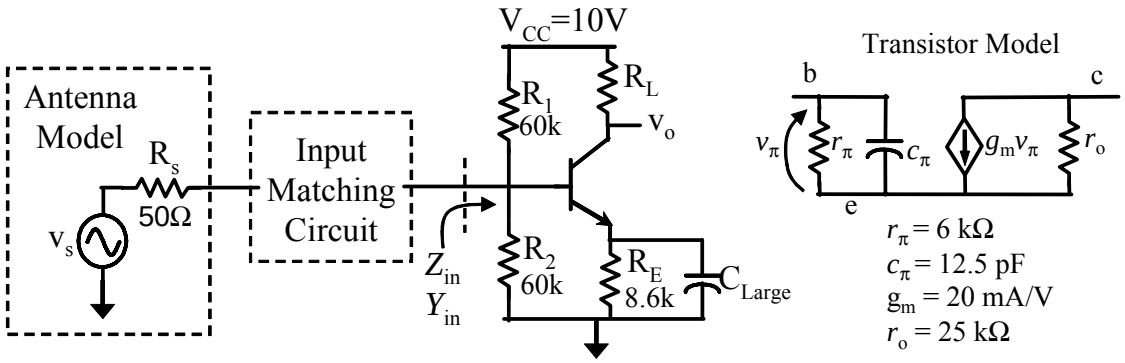


Figure 1

Question 3 Frequency Multiplier (Total 12 Marks)

The transistor in a class C frequency doubler conducts for 25ns then is off for 75 ns. The peak transistor current is 10 mA and the power supply is 5 V.

2 marks (a) What is the input frequency and what is the desired output frequency

4 marks (b) Find the average power supply current.

2 marks (c) Find the desired component of the output current.

4 marks (d) For approximately what range of load resistor values will the efficiency be over 25%?

Question 4 Mixer (Total 10 Marks)

5 marks (a) A mixer in a receiver has two inputs, the RF signal and the LO signal. For which input is linearity more important and why? A typical mixer as used in Lab 2 and shown in Figure 2 has two inputs, v_x and v_y. Which input is more linear? Very briefly explain why. Hence, which input should be used for the RF input and which for the LO input?

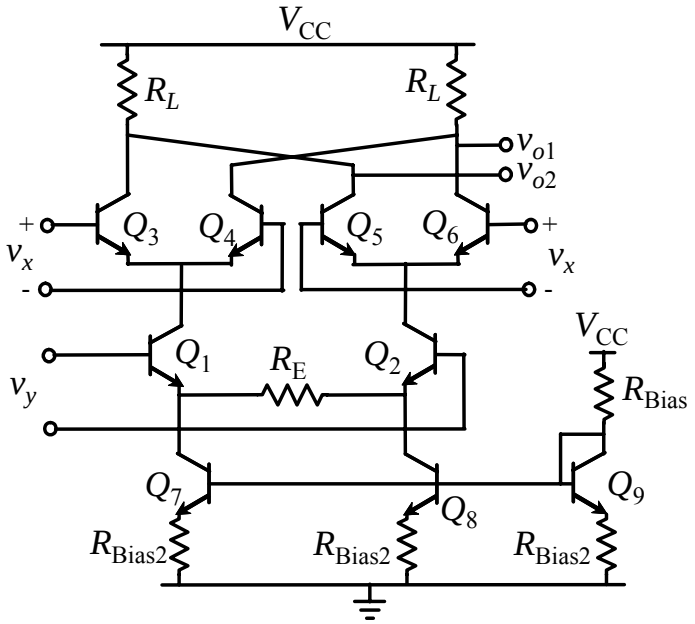


Figure 2

5 marks (b) The following waveform is a DSBSC with one sideband partially filtered out. Estimate the frequencies and amplitudes of the component signals and calculate the total rms output voltage.

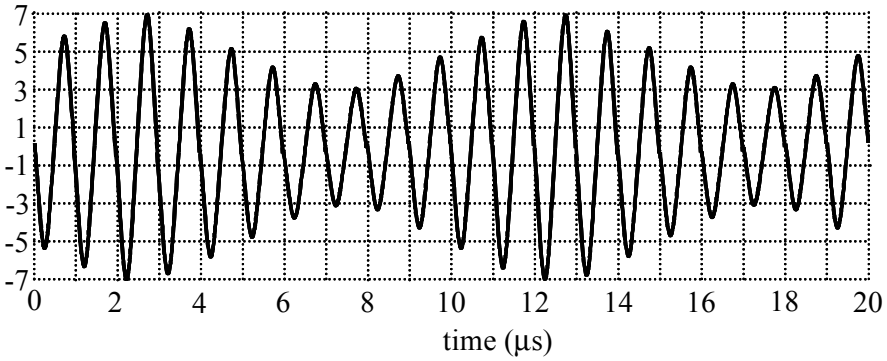


Figure 3

Question 5 Phase-Locked Loop (Total 20 Marks)

A PLL has $F(s)=\dfrac{1+s\times 4\times 10^{-5}}{s\times 10^{-3}}$, $K_{phase}=1\text{V/rad}$, and $K_{VCO}=1\times 10^{7}\,\text{rad/sec/V}$, and a divide-by-4 block between the VCO and the phase detector.

4 marks (a) Write the closed-loop transfer function $\theta_o(s)/\theta_i(s)$ in standard form (i) as an equation and (ii) with numbers.

4 marks (b) Determine ω_n and damping constant ζ. (Note, you cannot choose ζ, you must calculate it)

4 marks (c) For an input frequency step of 1 kHz, estimate the settling time and maximum phase error during the transient.

3 marks (d) For an input FM signal with a frequency deviation of 10 kHz, estimate the modulating frequency for which the phase error is maximum and the value of the phase error at that point.

5 marks (e) Sketch on a Bode plot the open loop gain and phase showing slopes, break points and approximate unity gain frequency. Comment on stability.

Question 6 Oscillator (Total 8 Marks)

An oscillator and its simplified small-signal model are shown in Figure 4. Note we have assumed that the two transistors have the same transconductance g_m.

3 marks (a) From the small signal model, write the expression for the open-loop gain.

2 marks (b) Apply the criteria for oscillation to solve for L for oscillation at 20 MHz.

2 marks (c) Determine the minimum value for g_m for sustained oscillations.

1 marks (d) Estimate transistor average bias current to result in this g_m.

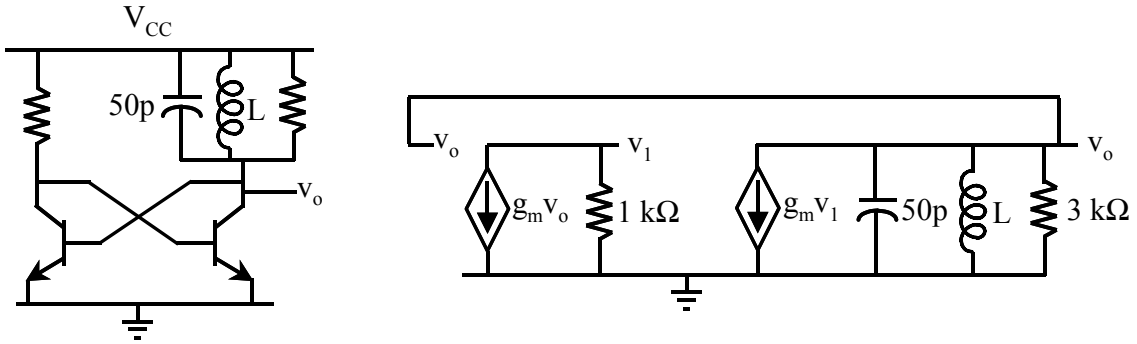


Figure 4

Final Exam 2006 Abbreviated Answers:

1 (a) figure including LO at 1015 MHz, image reject filter 902-928 MHz (center 915 MHz, BW 26 MHz), IF centered at 100 MHz, BW 1 MHz.
(b) Image at 1115 MHz. Origin: other signals, noise, distortion at input, removed by image reject filter.
(c) Output signal is 10^{-10} W and output SNR is about 21 dB.
(d) desired output is 10mV, simply the 1 mV multiplies by the desired linear gain of 10. Undesired gain required the solution of $(A\cos x + A\cos y)^3 = A^3(\cos^3 x + 3\cos^2 x \cos y + 3\cos x \cos^2 y + \cos^3 y)$. The second term is the one wanted and can be further exapanded as $3/2\ (1 + \cos 2x)(\cos y) = 3/2 \cos y + 3/4(\cos(2x-y) + 3/4(\cos 2x+y)$ where $x = (2\pi f_1 t)$ and $y = (2\pi f_2 t)$, where f_1 and f_2 are the two adjacent channels each at A = 100 mV. Thus, the two adjacent channels intermodulate with an amplitude of 10 x 3/4 x A^3 which is 7.5 mV.

2 (a) yin = 0.481m + j2.4m
(b) Series circuit: (from Zin) Rs = 80 Ohms, Cs = 0.397p. Parallel circuit: (from yin) Rp = 2079 Ohms, Cp = 0.382 pF.
(c) $N_2/N_1 = 6.45$, Req = 1040, Ct = 1.53 pF, Cadd = 1.15pF, L = 16.645 nH.
(d) iterate, need new values for N_2/N_1, Req, Ct, Cadd, L,
(e)(labeled (d)) need parallel C of 0.196 pF close to amplifier, then series L of 50.69 nH next to source.

3 (a) 10kHz, 20 kHz
b) theta = 60 degrees, Ip = 200 mA, Idc = 21.80 mA
c) I2 = 27.566 mA
d) efficiency = 17.4%

4 (a) RF linear, otherwise multiple input signals could intermodulate. LO can be nonlinear since it is a single frequency. Nonlinearity at the LO is in fact good, as switching helps to improve gain and noise performance. Linearity is achieved by adding degeneration resistor Re at the emitters of the RF input differential pair.
(b) Modulating signal at 50 kHz, Carrier at 400 kHz. Resultant signals at 350 kHz and 450 kHz with amplitudes of $4/\pi$ x 0.5 for bonus mark, 0.5 for full marks.
(c) Filter shape needed showing 0 dB gain at 450 kHz and -20 dB gain at 350 kHz. Resultant output at 0.5 and 0.05V (or actually at 4/pi x 0.5 and $4/\pi$ x 0.05). Time domain waveform showing peaks at 0.55 and valleys at 0.45 (actually, each is multiplied by $4/\pi$). Envelope is 100 kHz, waveform inside is at 450 kHz.

5. spectrum with carrier at 100 MHz, amplitude 1V. Sidebands at 99.975 MHz and 100.025 MHz both with amplitude of 0.2 V

6 (a) low-pass filter with phase lead correction, $F(s) = (1+s\tau_2)/s$
$\tau_2 = 1.59$ usec, $\tau_1 = 40.5$ usec.
(b) K = 16Mrad/sec, omega_n=628krad/sec, zeta=0.5
(c) peak error is $\pi/2$, max delta f = 285kHz, 2% tsettling = 12.74 usec
(d) Phase curve starting from -180 going to -90 going through -135 at 100 kHz. Since unity gain is shown occuring at 100 kHz, this is at -135, which means phase margin is 45

degrees, and this is stable. I note that the straight line approximation shows this point at unity, but the actual smoothed curve would show a gain slightly bigger than unity, hence the unity gain is slightly to the right, and phase margin is actually marginally bigger than 45 degrees.

7 (a) Ic about 1 mA, V_E = 1V, V_B=1.7V, V_C=5V
(b) L_2 C_2 C_3
(c) Frequency about 1MHz, $\beta > 10$. Since ft = 1 GHz and β is inversely proportional to frequency, (up to a limit of 100) at 1MHz, β is calculated to be 1000, so it has hit the limit of 100, which is clearly larger than 10, so the condition is met. Note, β is equal to 100 from DC up to 10 MHz.

Final Exam 2005 Abbreviated Answers

1(a) figure including LO at 4.9 GHz, input or image reject filter 5.15 to 5.25 GHz, IF filter centered at 300 MHz, BW = 10 MHz.
(b) Image at 4.6 GHz, other signals, noise, distortion at input, removed by image reject filter.
(c) IM3, best example inputs at 5.21, 5.22, IM3 at 5.20. Soln: Linear circuit.
(d) NF = 6 dB

2 (a) R_{eq} = 200Ω, C_{eq} = 7.958 pF, C_L = 7.858 pF, L = 3.183 nH, r_p = 1000Ω, R_L = 252.53Ω
(b) N_2/N_1 = 0.445. Gain = 4.45.
(c) Y_{in} = 0.580m + j 2.54122m, Z_{in} = 87.186 - j 377.8
(d) L = 46.05nH, C = 0.134 pF

3. (a) 100 kHz (equal to f_{in})
(b) I_{dc} = 2.592 mA
(c) I_1 = 4.435 mA
(d) R = 1317.8 Ohm

4. (a) Sketch waveform, and envelope of DSBSC signal. Spectrum tones at 50k, 70k, at 1V each. v_{rms} = 1V.
(b) Spectrum 50k at 0.1V, 70k at 1V. Time domain plot peak at 1.1, valley at 0.9, signal at 70k, envelope at 20k.

5. (a) nominal phase is 90 degrees, max phase offset is 90 degrees
(b) center frequency is 1.005 MHz. ζ = 0.707 (1 is also OK), ω_n = 50k to 80k (range of possible answers, depending on ζ and settling criteria. ω_n = 50k used in (c) to (e).)
(c) max error is 0.57 radian, peak error at 22 μsec
(d) B = 1.414 ω_n (from part b) This is the maximum frequency bandwidth for a modulated carrier to be transferred to the output.
(e) τ_1=6.366ms, τ_2=28.28 μsec. plot showing slope of 2, changing to slope of one at $1/\tau_2$, (35.36k), corresponding phase changing from -180 degrees to -90 degrees. Argument that unity gain occurs beyond $1/\tau_2$, e.g., using gain of line, and relative size of $1/\tau_2$ (35.36k) and ω_n (50k).

6. (a) sketch includes: base bias resistors, base decoupling capacitor, power supply, emitter resistor and RFC (or current source) to ground.
(b) at 1GHz, $\beta = 10$, set $C_2/C_1 = 5$. $C_1 = 6.079$ pF, $C_2 = 30.396$ pF.

7.

- Carrier is at 1MHz
- $\Delta f = 10$ kHz, $f_m = 33.33$ kHz, $\beta = 0.3$ these can be directly plugged into the equation
  $\cos \omega_c t - 0.15[\cos(\omega_c - \omega_m)t - \cos(\omega_c + \omega_m)t]$
- spectrum: 0.15 V at 0.9667 MHz, 1 V at 1 MHz, 0.15 V at 1.0333 MHz.
- $v_{rms} = 0.7228$ V.

Final Exam 2004 Abbreviated Answers

1. a), b), A transmitter where the input is at the IF fed into an image reject filter (which could be a simple lowpass filter) then into an up-conversion mixer, which is also fed by an LO at 2.65 Ghz, then into a power amplifier and antenna. Image reject filter at 200 MHz, BW is 1MHz, although simple lowpass filter cutting off somewhere beyond 200.5 MHz would also work. After the mixer is a bandpass filter letting the channel from 2.4 to 2.5 GHz.
..b) Image is at 5.1 GHz, from noise, harmonics, coupling.
c) intermodulation between two inband signals, resultant can be on top of the desired signal. Harmonics will be out of band. Example, 2.451 and 2.452 intermodulate to 2.450 GHz.
d) F = 10, NF = 10 dB

2. a) $y_{in} = 0.2m+j1.57m$, zin = 79.84+j626.8
b) $C_T = 15.915$ pF, $C_{add} = 3.415$ pF, $L = 3.98$ μH.
c) N2/N1 = 10
d) $R_L = 100$ Ohms
e) input matching, parallel C first of 3.34 pF, then series L of 3.96nH.

3. a) fin = 10MHz, Fout=20MHz
b) Idc=1.65 mA
c) theta=45 degrees, Ip=34.13 mA, I2 = 2.56 mA
d) R of 628.7 Ohms for 25% efficiency up to optimal resistance of 1.95k (which would result in 77.6% efficiency), past 1.95k, output voltage clips.

4.(a) RF needs to be more linear since RF signal has multiple frequencies, e.g., adjacent channels. If nonlinear, these could intermodulate and dump on top of the desired frequency. LO input has only 1 frequency (plus possibly harmonics). Nonlinearities will generate harmonics which are far away from the desired frequency. Note, since linearity for the LO is not very important, the LO input is often used to fully switch the transistors it is connected to - this is a highly noninear operation.
- Mixer vy input is more linear because of degeneration resistor RE. Input voltage is dropped across the combination of the nonlinear vbe junctions in series with RE, thus less goes across vbe, hence bigger signal can be applied.

- Conclusion, RF applied to bottom diff pair, (vy input), LO applied to upper quad (sometimes called switching quad) (vx input).

(b) two signals A and B at output with amplitudes 5 and 2 (peak is 5+2=7 and valley is 5-2=3). High frequency component is the big signal at 1 cycle per μsec or 1MHz. Ripple shows difference frequency or 100 kHz. Thus, 5V at 1MHz and 2V at 0.9 MHz (or it could be 2V at 1.1 MHz, but not both 0.9 and 1.1). Note, 1 MHz is not the carrier frequency but one of the sidebands, since this is DSBSC where SC stands for suppressed carrier. Total RMS voltage is the square root of the sum of the rms voltage squared, or 3.808V.

5. a) $\frac{\theta_o}{\theta_i} = \frac{K}{\tau_1}\frac{(s\tau_2+1)}{s^2 + s\frac{K\tau_2}{\tau_1} + \frac{K}{\tau_1}} = 2.5\text{G}\frac{s\times 400\mu + 1}{s^2 + s\times 100\text{k} + 2.5\text{G}}$ where $K = \frac{K_{VCO}K_{Phase}}{N}$

b) ω_n = 50k rad/sec, ζ = 1.

c) settling time t = 100μsec to 160μsec, error_max = 0.0465 radians.

d) Maximum error occurs when $\omega_m = \omega_n$ = = 50k rad/sec. At $\omega_m = \omega_n$ = 50k rad/sec the output phase error is 0.628 radians.

e) Low frequency slope of -2 (-40 dB/decade) up to $\omega = 1/\tau_2$ then a slope of -1. Low frequency phase is -180, then heads to -90 crossing through -135 at $\omega = 1/\tau_2$. For stability, note low frequency line with a slope of -2 is a plot of $K/(\tau_1\,\omega^2) = \omega_n^2/\omega^2$. This equals 1 at $\omega = \omega_n$ from above = 50k. Solve $1/\tau_2$ = 25krad/sec. Since unity point is beyond the break point, phase shift is less than -135 and system is stable.

6. gain blocks are: -gm x 1k, and tuned amp with gain gm/Y where Y is 1/3k + jωC -j/(ωL)

..b)Multiply these two blocks, equate to 1 +j0, imaginary: L = $1/(\omega^2$ x C) = 1.2665 μH. (Note, that this is equivalent to X1 + X2 + X3 = 0 except that there are only two reactive components resonating so one of them is already equal to zero.)

c) real: -gm x 1k x -gm x 3k = 1. result, g_m = 0.577 mA/V.

d) gm = Ic/Vt where Vt = 25 mV. Result, Ic = 14.43 uA.

Final Exam 2003 Abbreviated Answers

1. General Receiver 20 Marks

a) sketch of LNA, image reject filter, mixer, IF filter. LO at 5.5GHz, Image reject filter has 200 MHz bandwidth, centre at 5.2 GHz, IF filter has BW of 1 MHz, centre at 300 MHz.

b) Image at 5.8 GHz due to other signals or noise at input, removed by image reject filter

c) adjacent channels at 5.201, 5.202, 5.203, ...5.300 and 5.199, 5.198, 5.197, ... 5.100. Removed by IF filter.

d) answer 2.09 or 3.20 dB

2. Tuned Amplifier 20 Marks

a) Y_{in} = 0.333m + j3.30m, Zin = 30.297 - j300, Yin is more appropriate for parallel matching, Zin is more appropriate for series matching, with transformers you pretty well only need the component values.