ELEC4705 – Fall 2009

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LECTURE 16
The MOSFET

Contents

16.1. Introduction to MOSFET

The MOSFET (Metal Oxide Silicon Field Effect Transistor) is a device that controls a current between two contacts (Source and Drain) using a voltage contact (Gate). The device uses a surface effect to create a n-type region in a p-type substrate (or the converse). To understand this we take a simple capacitor structure using a p-type substrate a oxide layer and a metal gate, as shown in figure 1. If we apply a positive potential to the gate (the substrate is grounded) electrons will be attracted to the gate and will pile up at the surface underneath the gate.

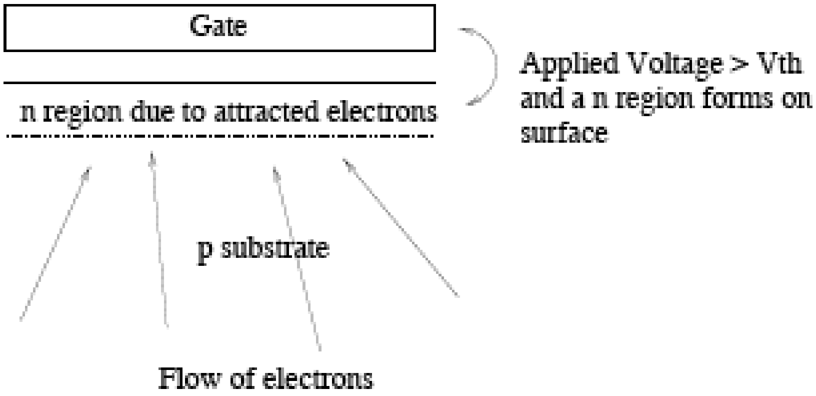


Figure 1. A Cap Structure

At some voltage V_{th} called the threshold voltage the region under the gate will have enough additional electrons that $n > p$ and the material will be $n - type$ not $p - type$. The oxide is very important as it stops the current flow towards the gate and forces the electrons to *"pile up"* underneath the gate and turn the material to be $n - type$.
The basic MOSFET structure uses the capacitor structure with $n{-}type$ regions placed at either edge, known as the source and drain, see figure 2.

16.1.1. Basic Channel Physics

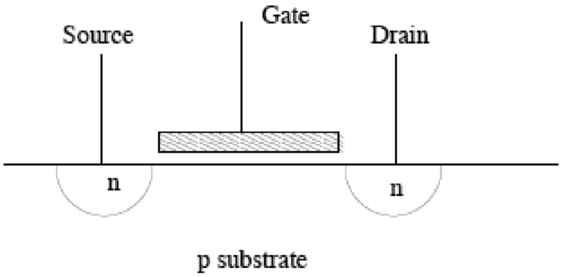
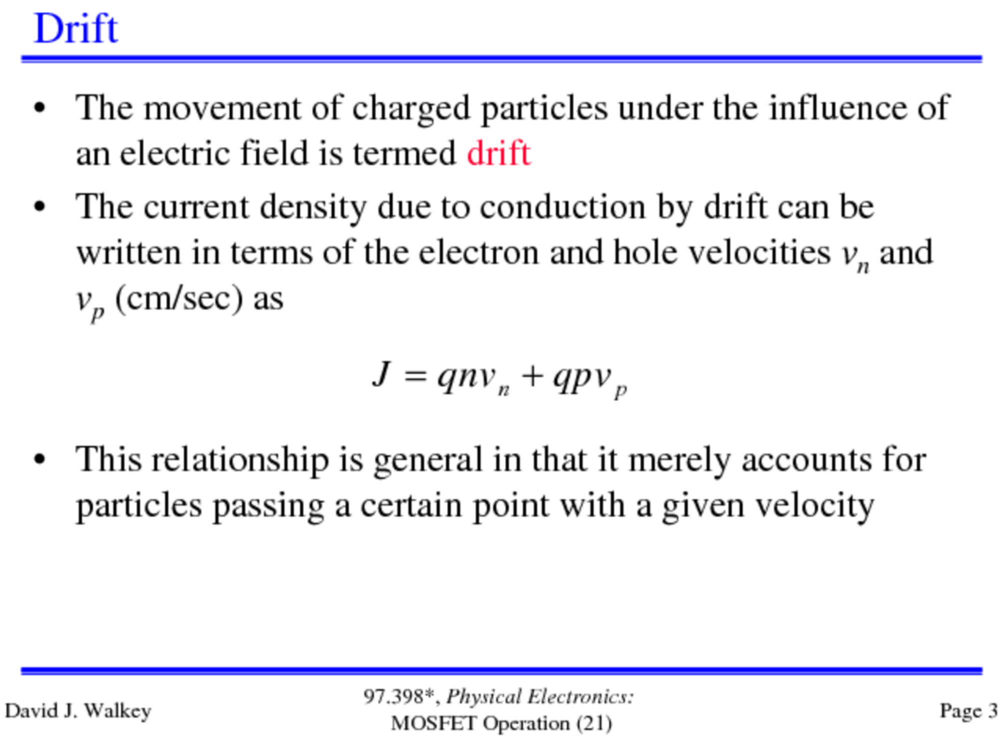


Figure 2. A MOS Structure



Drift

- The movement of charged particles under the influence of an electric field is termed drift
- The current density due to conduction by drift can be written in terms of the electron and hole velocities v_n and v_p (cm/sec) as

$$J = qnv_n + qpv_p$$

- This relationship is general in that it merely accounts for particles passing a certain point with a given velocity

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97.398*, *Physical Electronics:*
MOSFET Operation (21)

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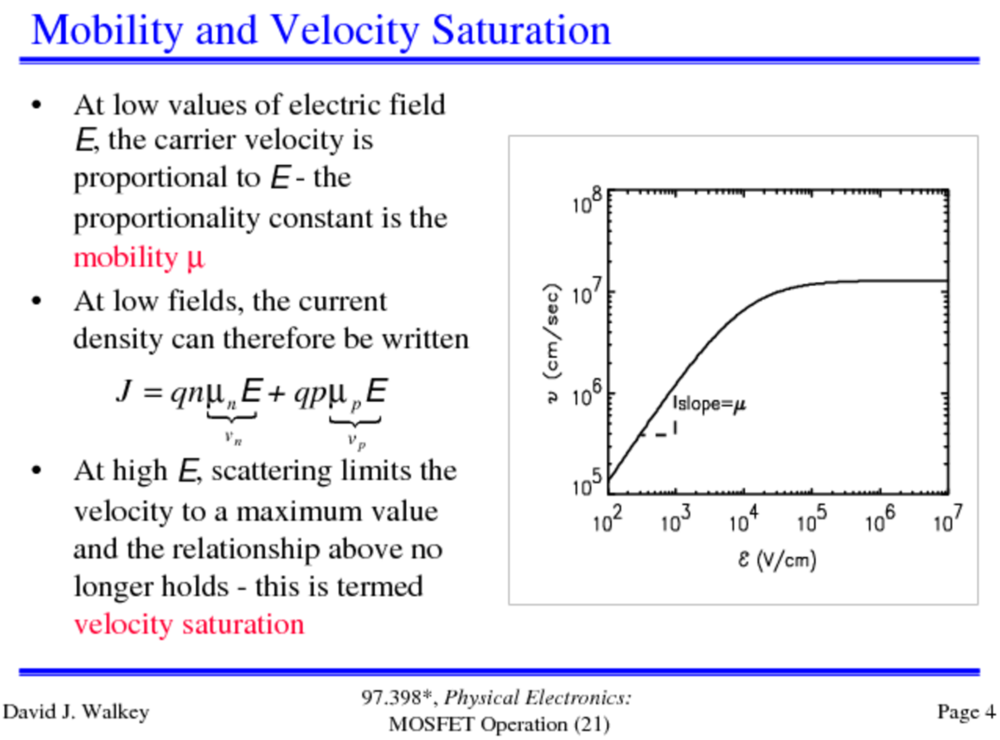

Mobility and Velocity Saturation

- At low values of electric field E, the carrier velocity is proportional to E - the proportionality constant is the mobility μ
- At low fields, the current density can therefore be written

$$J = qn\underbrace{\mu_n E}_{v_n} + qp\underbrace{\mu_p E}_{v_p}$$

- At high E, scattering limits the velocity to a maximum value and the relationship above no longer holds - this is termed velocity saturation

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Factors Influencing Mobility

- The value of mobility (velocity per unit electric field) is influenced by several factors
  - The mechanisms of conduction through the valence and conduction bands are different, and so the mobilities associated with electrons and holes are different. The value for electrons is more than twice that for holes at low values of doping
  - As the density of dopants increases, more scattering occurs during conduction - mobility therefore decreases as doping increases
  - At low temperatures, electrons and holes gain more energy than the lattice with increasing T, therefore mobility increases. At high temperatures, lattice scattering dominates, and thus mobility falls
  - Conduction through bulk material (diodes, BJTs) experiences less scattering than conduction along a surface (MOSFET), hence bulk mobility is higher than surface mobility (see Table 21.1)

Resistivity and Conductivity

- The expression for J in terms of μ and E can be written as

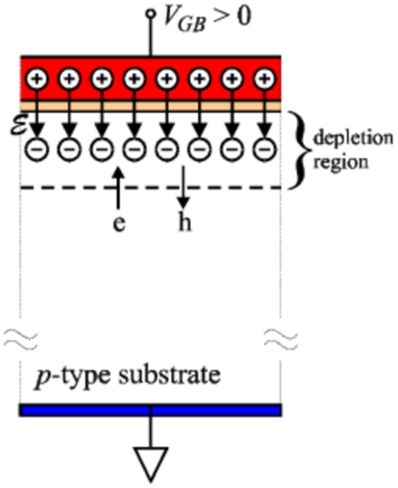
$$J = (qn\mu_n + qp\mu_p)E$$

- The first term is the conductivity σ, in $(\Omega\text{cm})^{-1}$, and its inverse is the resistivity ρ, already used in the calculation of series resistance in the diode structure

$$\sigma = \frac{1}{\rho} \equiv qn\mu_n + qp\mu_p$$

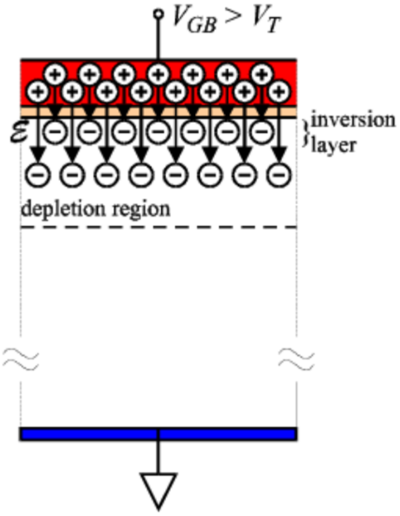
MOS Structure in Depletion

- A +ve V_{GB} applied to the gate of a MOS structure whose substrate is grounded produces E penetrating into the substrate
- For a *p*-type substrate, E repels majority holes from the surface, creating a depletion region
- Some minority electrons are attracted to the surface, but at low values of V_{GB} their numbers are not sufficient to cause much effect
- Charge balance is primarily +ve holes on gate, -ve ionized acceptors
- This is termed depletion operation



MOS Structure in Inversion

- At large V_{GB}, a dense inversion layer of electrons forms under the surface
- Further increases in V_{GB} only change the density of the inversion layer
- The potential at which the inversion layer dominates the substrate behaviour is the threshold voltage V_T
- This inversion layer will form the conductive channel between the source and drain of the MOSFET



16.1.2. MOSFET Operation

The basic operation of the device is to bias the gate with $V_G > V_{th}$ and form a $n - type$ region between the source and the drain. This provides a simple $n - type$ path between the $n - type$ source and drain regions for electrons to flow. This region is called a channel. Note that without forming the channel there are two back to back diodes formed which will not allow appreciable current to flow. The formation of this channel provides a simple resistive path between the source and the drain. The thickness of the channel is function of the difference between the gate potential and the potential in the substrate near the surface.

We can place a voltage between the source and the drain and cause a current to flow. Typically we ground the source and bias the drain with V_{ds}. The ability to change the thickness of the channel using the gate potential provides a means of controlling the current from the source to the drain. We basically can form a voltage controlled resistor.

One thing to note is that the appliction of a drain voltage raises the potential of the region of the substrate at the surface near the drain. This results in a thinner channel at that end as shown inf figure 3 (as the gate to substrate potential is reduced).

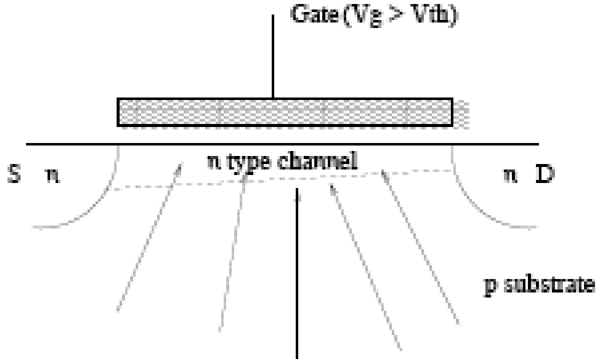
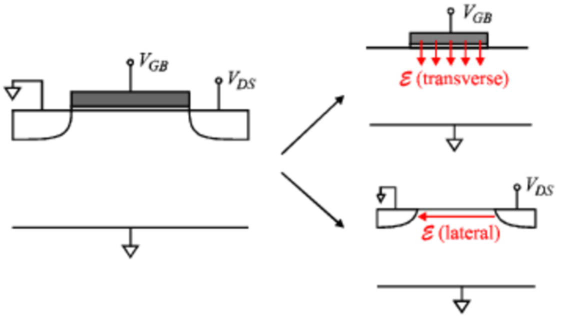


Figure 3. Channel formation of a MOSFET

Electric Fields in the MOSFET

- Two distinct electric field distributions exist in the MOSFET structure
  - The transverse field is caused by the potential difference between the conductive gate and the substrate. This field is supports the substrate depletion region and inversion layer
  - The lateral field arises due to a non-zero source to drain potential, and is (in the simple model) the main mechanism for current flow in the MOSFET

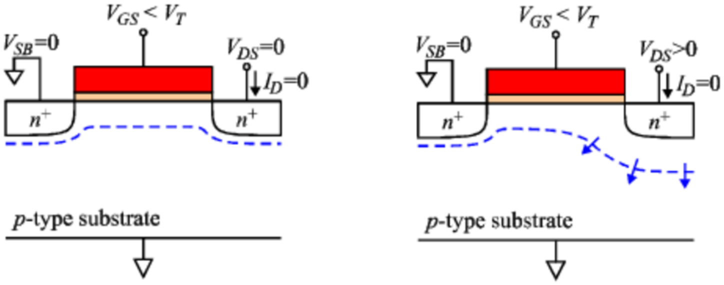


Qualitative MOSFET Operation

- Assume an n-channel MOSFET, i.e. n^+ source and drain regions in a uniformly doped p-type substrate
- Source and substrate are grounded
- Results discussed here apply to p-channel (n-type substrate) devices with reversal of polarities

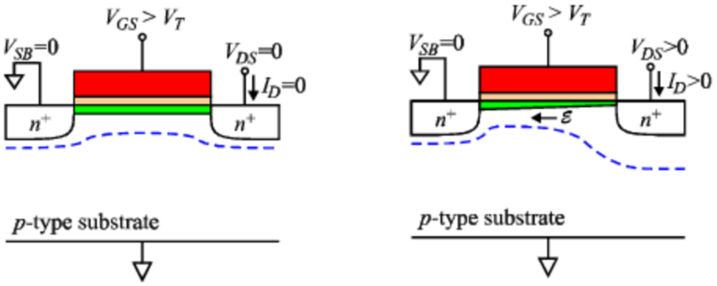
n-Channel MOSFET With $V_{GS} < V_T$

- With $V_{GS} < V_T$, there is no inversion layer present under the surface
- At $V_{DS} = 0$, the source and drain depletion regions are symmetrical
- A positive V_{DS} reverse biases the drain substrate junction, hence the depletion region around the drain widens, and since the drain is adjacent to the gate edge, the depletion region widens in the channel
- No current flows even for $V_{DS} > 0$, since there is no conductive channel between the source and drain for $V_{GS} < V_T$



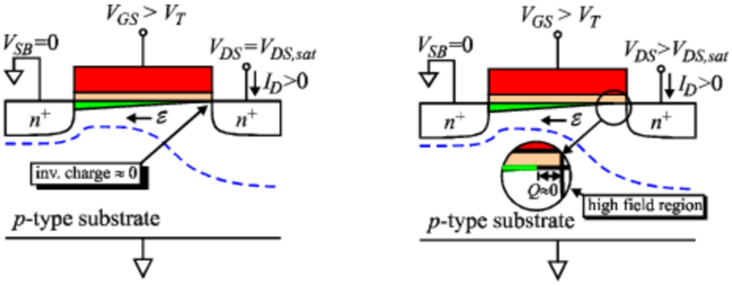
n-Channel MOSFET With $V_{GS} > V_T$, small V_{DS}

- With $V_{GS} > V_T$, a conductive channel forms under the surface - a non-zero transverse field is present
- I_D is zero for $V_{DS} = 0$ since no lateral field is present
- For $V_{DS} > 0$, transverse E is present and current flows
- The increased reverse bias on the drain substrate junction in contact with the inversion layer causes inversion layer density to decrease



n-Channel MOSFET With $V_{GS} > V_T$, large V_{DS}

- The point at which the inversion layer density becomes very small (essentially zero) at the drain end is termed pinch-off
- The value of V_{DS} at pinchoff is denoted $V_{DS,sat}$
- Past pinchoff, further increases in lateral electric field are absorbed by the creation of a narrow high field region with low carrier density ($J_n = qn\mu_n\mathcal{E}$, so if n is small $\mathcal{E}$ is large)



MOSFET Regions of Operation

- There are three regions of operation in the MOSFET
  - When $V_{GS} < V_T$, no conductive channel is present and $I_D = 0$, the cutoff region
  - If $V_{GS} < V_T$ and $V_{DS} < V_{DS,sat}$, the device is in the triode region of operation. Increasing V_{DS} increases the lateral field in the channel, and hence the current. Increasing V_{GS} increases the transverse field and hence the inversion layer density, which also increases the current
  - If $V_{GS} < V_T$ and $V_{DS} > V_{DS,sat}$, the device is in the saturation region of operation. Since the drain end channel density has become small, the current is much less dependent on V_{DS} , but is still dependent on V_{GS}, since increased V_{GS} still increases the inversion layer density

16.2. Pinch Off

A new condition arises if we increase the drain voltage substantially i.e. $V_{DS} > V_{DS_{sat}}$ (where $V_{DS_{sat}}$ is called the saturation voltage). The drain voltage becomes large enough that the gate to substrate potential at the drain is smaller than threshold. Therefore the channel thickness at this end goes to zero. We call this *pinch off*. Electrically, the effect of pinch off is that the channel no longer acts like a simple resistor. The current I_{DS} becomes fixed (saturated) at the value just prior to pinch off, shown inf figure 4.

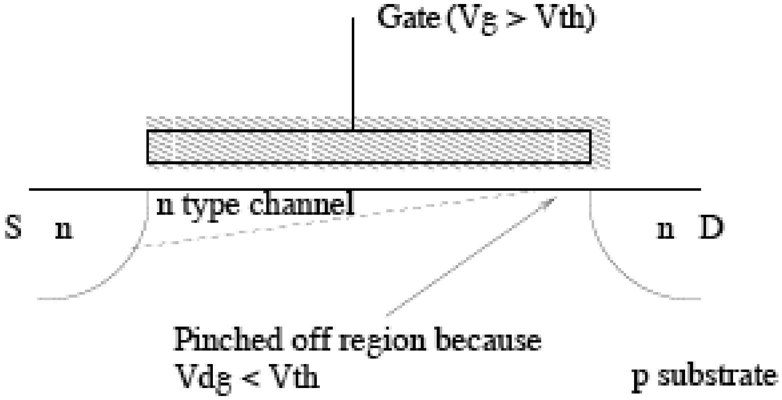
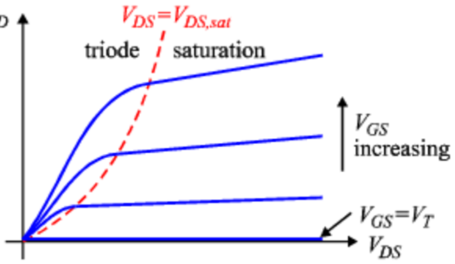


Figure 4. Pinch Off

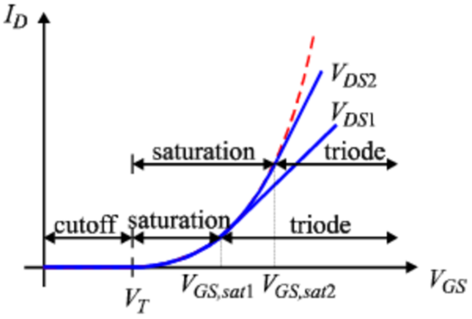
MOSFET I_D-V_{DS} Characteristic

- For $V_{GS} < V_T$, $I_D = 0$
- As V_{DS} increases at a fixed V_{GS} , I_D increases in the triode region due to the increased lateral field, but at a decreasing rate since the inversion layer density is decreasing
- Once pinchoff is reached, further V_{DS} increases only increase I_D due to the formation of the high field region
- The device starts in triode, and moves into saturation at higher V_{DS}



MOSFET I_D-V_{GS} Characteristic

- As I_D is increased at fixed V_{DS}, no current flows until the inversion layer is established
- For V_{GS} slightly above threshold, the device is in saturation since there is little inversion layer density (the drain end is pinched off)
- As V_{GS} increases, a point is reached where the drain end is no longer pinched off, and the device is in the triode region
- A larger V_{DS} value postpones the point of transition to triode



16.2.1. MOSFET Equations

The Triode Region: $V_{GS} > V_{th} \quad , \quad V_{DS} < V_{DS_{sat}}$

$$I_{DS} = I_0[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{16.1}$$

The $V_{DS}^2/2$ *term takes the narrowing of the channel at the gate region into account as* V_{DS} *approaches* $V_{DS_{sat}}$.

The Saturation Region: $V_{GS} > V_{th} \quad , \quad V_{DS} > V_{DS_{sat}}$

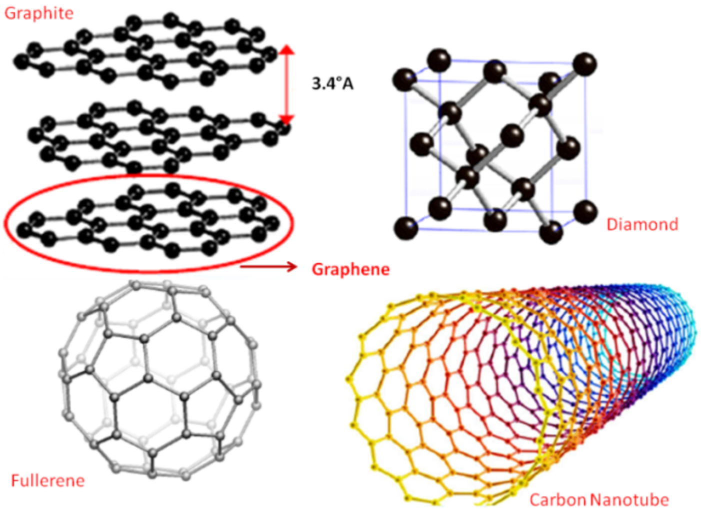
$$V_{DS_{sat}} = V_{GS} - V_{th} \tag{16.2}$$

$$I_{DS} = I_0\frac{(V_{GS} - V_{th})^2}{2} \tag{16.3}$$

In saturation mode the MOSFET acts like a nonlinear voltage controlled current.

16.3. Other FET structures

16.3.1. Carbon Nanotube FETS



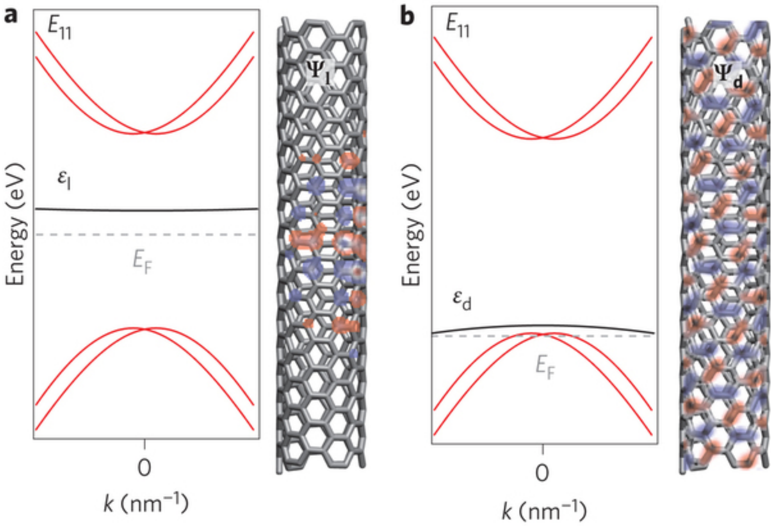
Carbon comes in a number of forms:

Diamond: Bulk crystal – standard band structure, insulator due to large bandgap.

Graphite/Graphene: 2D sheets of carbon in hexagonal arrangement. 2D Crystal bonded by weak forces. Cool band structure with very low mass electrons.

Fullerene/BuckyBalls: Soccer ball like structure. Band structure determined by size. Small number of atoms so bands with finite (small) number of states.

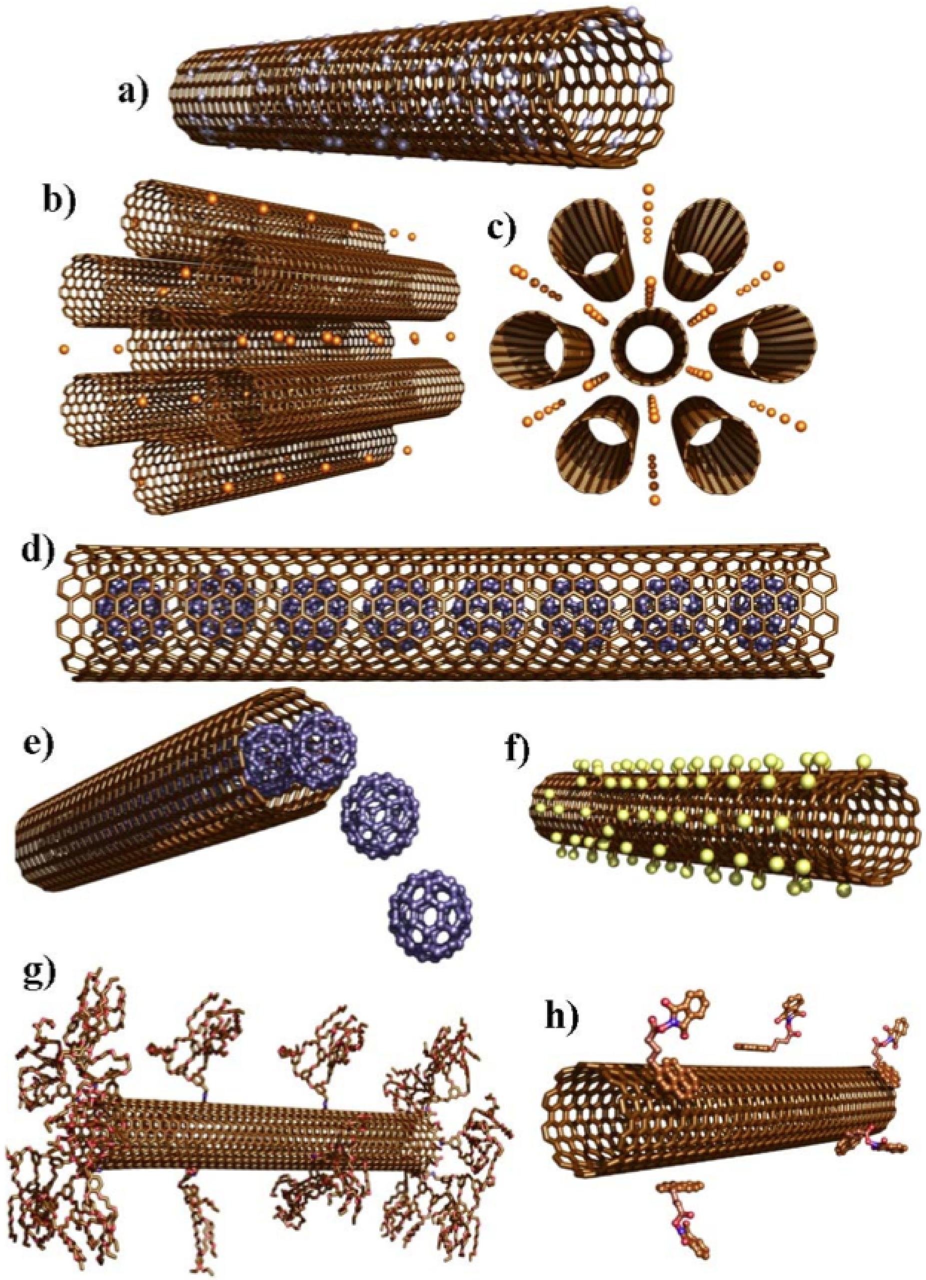
Nanotubes: Tube like extension of BuckyBalls or a wrapped graphene layer. Band structure of bands with small number of states. Twist/radius determines band-gap (Metal/Insulator/Semiconductor). High electron mobility. Very strong and hard. Can be doped in many ways.



Nanotubes can be created using chemistry.

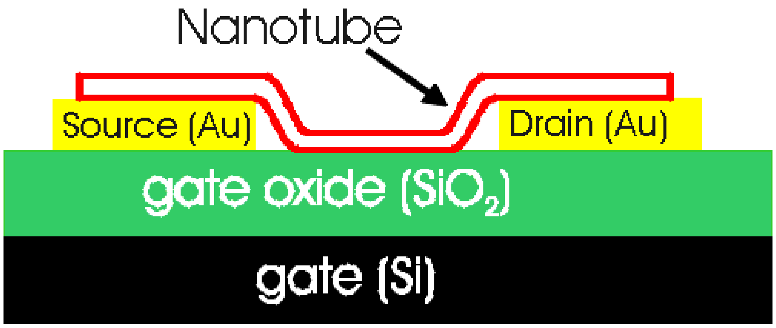
Fermi level: E_f can be changed by doping with impurities or molecular attachment.

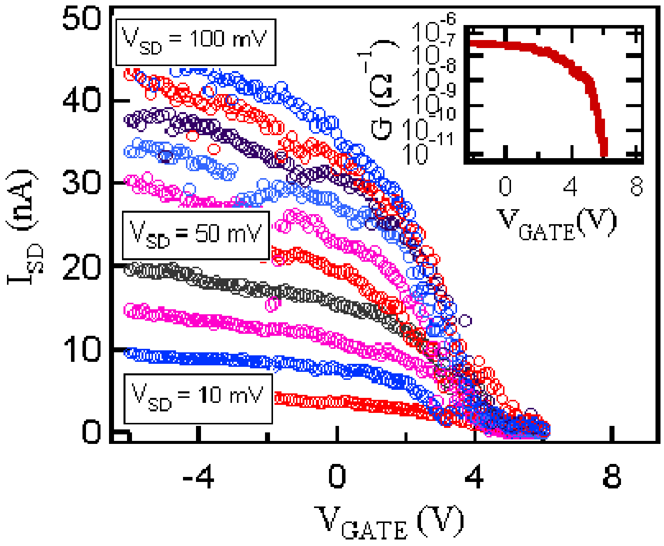
Versatile: Many sizes and configurations with a wide variety of electronic and optical properties.



Doping can be done in many ways!

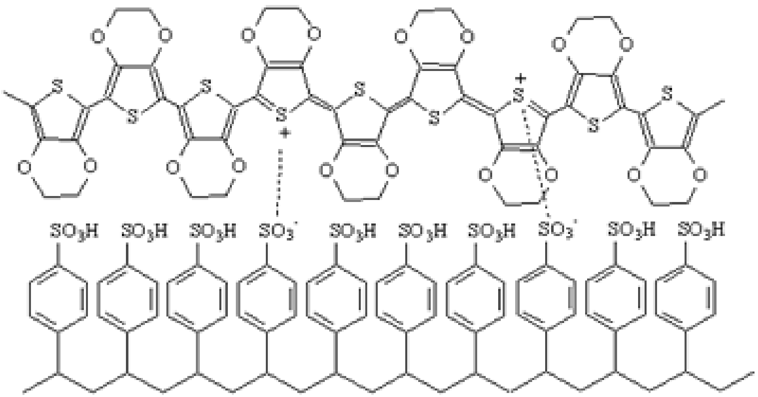
IBM very recently announced a new method of fabricating circuits of FET devices based on nanotube devices. 10,000 working devices on a chip.

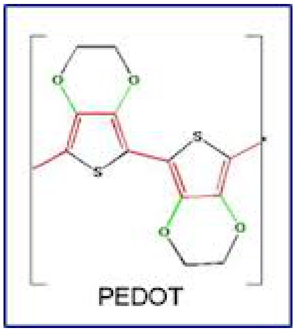


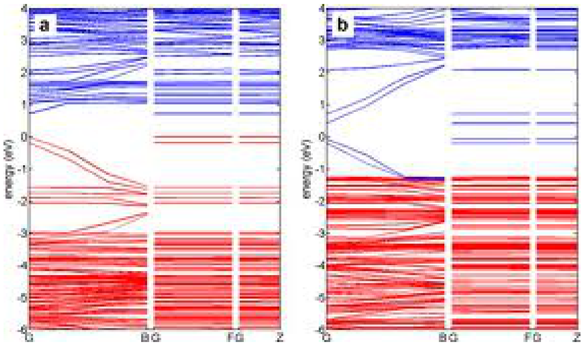


Simple device but with potentially very high speeds and densities.

16.3.2. Polymer Based FETS

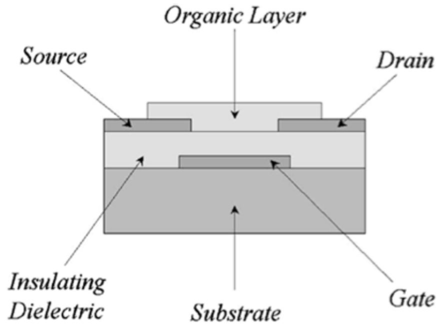






Polymers such as PEDOT are semiconductors.

- **Crystal:** 1D crystal along the polymer. De-localized electrons that conduct. Band structure with gaps and bands with a finite number of states.
- **Doping:** Can be doped with impurities to produce N and P type materials.



Devices: Create a standard type FET.
Performance: Very slow. Mobilities are much lower.
Price: Very low printable electronics.
Size: Much larger.
Optical?: Can be made optical active
Stability: Lots of questions?