Final Exam

Sample Final Exam

ELEC-5801: High-Speed and Low-Power VLSI

Department of Electronics, Carleton University

Instructor:	Maitham Shams	**Exam Duration:**	3 hours
Booklets:	None	**Number of Pages:**	9 with this
Aids Allowed:	Scientific Calculator	**Number of Students:**	7

Last Name: _____

First Name: _____

ID: _____

Q1	Q2	Q3	Q4	Q5	Total
/30	/20	/15	/15	/20	/100

Formula and Data

$$
\begin{aligned}
I_n(\text{sat}) &= 400\frac{W}{L}(V_{GS}-V_{TN})^{1.30} \quad \mu\text{A} \\
I_p(\text{sat}) &= 150\frac{W}{L}(V_{GS}-V_{TP})^{1.50} \quad \mu\text{A} \\
V_{DD} &= 1 \text{ V} \\
V_{TN} &= 0.40 \text{ V} \\
V_{TP} &= 0.35 \text{ V} \\
L_{\text{min}} &= 90 \text{ nm} \\
t_{ox} &= 25 \text{ nm} \\
\epsilon_{ox} &= 3.9 \times 8.854 \times 10^{-14} \quad \text{F/cm}
\end{aligned}
$$

[1] True or False **(30 marks, 0.5 each)**

1. At 100 MHz, the power dissipation of a modern MCML circuit is lower than its conventional CMOS version. ☐ True ☐ False
2. In α-power law, $\alpha = 2$ for long channel devices. ☐ True ☐ False
3. Dynamic CMOS circuits usually don't have short-circuit energy dissipation. ☐ True ☐ False
4. Abstraction is a powerful technique commonly applied in analog circuit design. ☐ True ☐ False
5. Dynamic circuits have to maintain a minimum clock frequency to avoid losing data. ☐ True ☐ False
6. Small voltage swing is a major factor for the superiority of MCML gates in speed compared to conventional CMOS gates. ☐ True ☐ False
7. An asynchronous circuit always consumes less energy than its synchronous counterpart. ☐ True ☐ False
8. In a multi-V_T digital circuit, the critical path uses low-V_T transistors. ☐ True ☐ False
9. When a static logic gate is not switching, there is always a path connecting the output to the power supply or ground. ☐ True ☐ False
10. Progressive transistor sizing improves speed of a fabricated IC by 10% or more. ☐ True ☐ False
11. Speed-independent circuits function correctly regardless of wire delays. ☐ True ☐ False
12. A disadvantage of dynamic CMOS circuits is that they produce glitches. ☐ True ☐ False
13. In a pseudo-NMOS logic gate, the lower the load resistance, the higher the nominal output low, V_{OL}. ☐ True ☐ False
14. Higher speed is always associated with higher power consumption. ☐ True ☐ False
15. A PTL circuit usually has a higher device count compared to it conventional CMOS counterpart. ☐ True ☐ False
16. Tree-like structures are generally less prone to glitches than chain-like structures. ☐ True ☐ False
17. The input resistance of an ideal logic gate is zero. ☐ True ☐ False
18. EMI is higher in an asynchronous circuit compared to its synchronous version. ☐ True ☐ False
19. Pre-computation is a proven power-reduction technique for comparators. ☐ True ☐ False
20. A limitation of the basic domino CMOS circuits is that they can only implement non-inverting cascaded functions. ☐ True ☐ False
21. pipelining a circuit reduces its latency. ☐ True ☐ False

22. In conventional CMOS circuits all of the energy eventually goes to ground. ☐ True ☐ False

23. The smaller the gate-oxide thickness, the lower the delay. ☐ True ☐ False

24. Electron mobility is a constant factor in modern CMOS IC circuits. ☐ True ☐ False

25. DCVSL is a ratio-less CMOS logic style. ☐ True ☐ False

26. Clock skew is becoming less of a problem by increasing integration density. ☐ True ☐ False

27. The overlap gate-source and gate-drain capacitances experience Miller Effect during switching. ☐ True ☐ False

28. The goal of parallelism is to sacrifice area for reducing power consumption or increasing speed. ☐ True ☐ False

29. The lower the slope of the input to a CMOS inverter, the higher the short-circuit energy dissipation. ☐ True ☐ False

30. In deep saturation, the effective channel length is shorter than the physical distance between the source and drain of a MOSFET. ☐ True ☐ False

31. The diffusion capacitances in a CMOS circuit may be ignored in calculating the delay, because the gate-oxide capacitances are much larger. ☐ True ☐ False

32. Leakage current through the gates of MOSFETS increases as the gate-oxide thickness reduces. ☐ True ☐ False

33. Any MOSFET with a feature length below a micron is considered a short-channel device. ☐ True ☐ False

34. Driving a large load in one stage is faster than driving it through two stages. ☐ True ☐ False

35. An XOR gate is considered delay insensitive the way it is normally operated in synchronous circuits. ☐ True ☐ False

36. In an 8-input conventional CMOS NAND gate, the NMOS transistor closest to the output usually has the highest V_T. ☐ True ☐ False

37. In using multiple or dual supplies the designers attempt to equalize the delays through the different paths. ☐ True ☐ False

38. The maximum value of a reversed-biased diffusion capacitance is when the applied potential across it is closer to zero. ☐ True ☐ False

39. An n-input NAND gate has a lower logical effort than an n-input NOR gate. ☐ True ☐ False

40. In an ideal logic gate the low and high noise margins are both zero. ☐ True ☐ False

41. In DCVSL circuits, the rising delay is always larger than falling delay. ☐ True ☐ False

42. Last-arriving inputs should be connected to the transistors attached to the power rails (i.e. GND and V_{DD}). ☐ True ☐ False

43. A multiplier is usually more power consuming than several adders with the same input sizes. ☐ True ☐ False

44. The static operation of a conventional CMOS logic gate depends on its fan-out. ☐ True ☐ False

45. Delay of N serially connected MOSFETs increases quadratically with N. ☐ True ☐ False

46. CPL logic gates need a couple of PMOS transistors to produce full-swing outputs. ☐ True ☐ False

47. A level-restorer is needed when a circuit using a higher V_{DD} connects to a circuit with a lower V_{DD}. ☐ True ☐ False

48. When driving a very large capacitance it is better to use a tri-state buffer with a single stack of transistors at the output rather than a double stacked one. ☐ True ☐ False

49. Since MOSFET is a symmetric device, its source and drain terminals are identified by their relative voltage potentials. ☐ True ☐ False

50. Power dissipation remains almost constant in fixed-voltage technology scaling. ☐ True ☐ False

51. In saturation mode, MOS current is totally independent of source-to-drain potential. ☐ True ☐ False

52. Dynamic power dissipation of MCML gates increases linearly with frequency. ☐ True ☐ False

53. Scaling both V_{DD} and V_T doesn't affect static power dissipation. ☐ True ☐ False

54. Short-channel devices have wider saturation region (in I-V curve) compared to long-channel devices operating within the same permissible voltage range. ☐ True ☐ False

55. Charge-sharing is more of a problem in a dynamic CMOS gate with a large output capacitance compared to its internal node capacitances. ☐ True ☐ False

56. Lower power dissipation is a definitive advantage of asynchronous circuits. ☐ True ☐ False

57. If used for short-channel devices, Shockley's square law over-estimates the current . ☐ True ☐ False

58. By enlarging the sizes of the logic gates along a path, the overall delay decreases. ☐ True ☐ False

59. It is impossible to implement a non-inverting function of the the primary inputs in one stage using conventional CMOS style. ☐ True ☐ False

60. Reducing the threshold voltage in digital CMOS circuits improves speed and reduces static power dissipation. ☐ True ☐ False

[2] General Delay and Power Calculations **(20 marks)**

1. A two-input NAND gate in 90 nm technology that drives a 100 fF load in 50 ps, with equal rising and falling delays.

   (a) Design this logic gate, i.e. find transistor sizes.

   (b) What is the maximum frequency of operation while maintaining a full-swing output?

   (c) What is the capacitive load at each input of this logic gate?

2. A CMOS chip fabricated in 90 nm technology operates at a maximum frequency of 3 GHz and dissipates 5 w with V_{DD} =1 V. The very same chip is then scaled-down and fabricated in 65 nm technology with V_{DD} =0.9 V.

   (a) What is the maximum frequency of operation, approximately?

   (b) What is the power dissipation, approximately?

[3] CMOS Logic Styles **(15 marks)**

Consider the following Boolean function $Z = \overline{AB + DE + C(AE + DB)}$.

1. Implement in Conventional CMOS logic style with minimum number of transistors.

2. Implement in PTL with full-swing output.

[4] Delay Optimization (Logical Effort) **(15 marks)**

A 6-input OR gate receives its input from an inverter and drives a capacitive load. The ratio of the output load to the input capacitance of the inverter is H. Which of the following two configurations for implementing this logic gate is better in terms of delay.

1. Input Inverter + (6-input NOR + Inverter) + Load

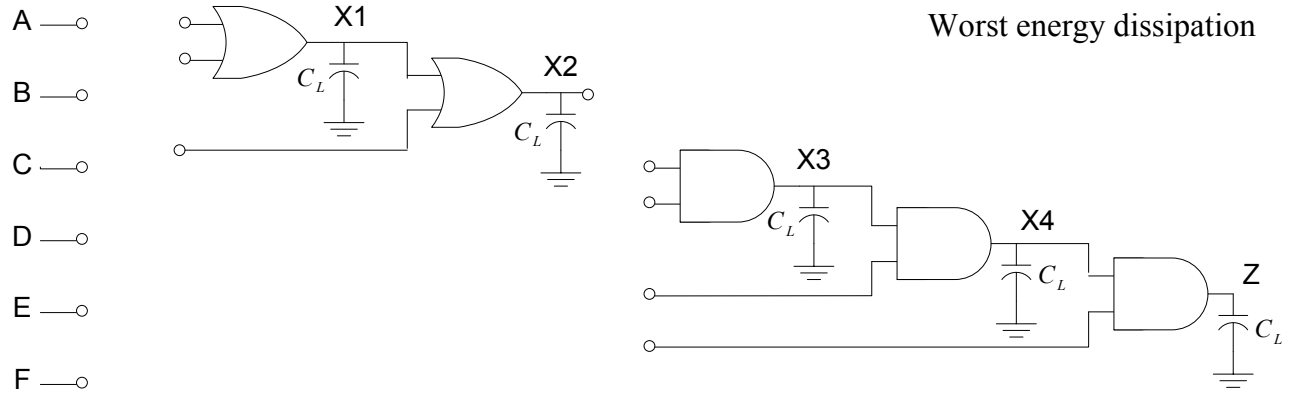
2. Input Inverter + (3-input NOR + 2-input NAND) + Load

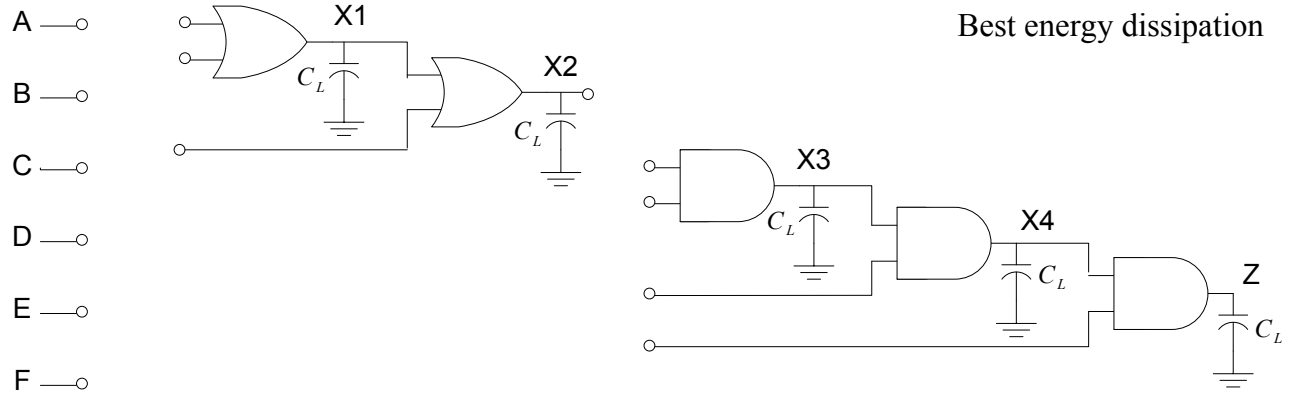
[5] Power Optimization (Switching Activity) **(20 marks)**

John wants to implement the function in the next pages with the given input probabilities. Mike sees the circuit and tells mike that you have wired the gates such that it consumes the highest possible energy. Then Mike shows John how to do the wiring to minimize the energy consumption. On the figures show how John connected the inputs and the gates, and how Mike fixed it. Next calculate the energy savings by using Mike's method compared to John's by filling the table and the corresponding box. Finally write what general rule or rules Mike used to achieve the energy savings. Note that all internal nodes and the output have the same load capacitance and all other factors are ignorable. Use this page for your rough work.

Z=(A+B+C)(DEF)

Input	A	B	C	D	E	F
P_1	0.3	0.5	0.8	0.7	0.4	0.2





Node	Worst Case P_0	Worst Case P_1	Worst Case α	Best Case P_0	Best Case P_1	Best Case α
X1						
X2						
X3						
X4						
Z						

$$E_{Saved} = \frac{E_{Best} - E_{Worst}}{E_{Worst}} =$$

What is(are) the rule(s) to be used for lowest energy dissipation?

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