Assignment 4, Due 25 April 2016

ELEC-5801: High-Speed and Low-Power VLSI

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Use the 65 nm CMOS technology kit with $V_{DD} = 1.0$ V . Implement a 4-bit Ripple-Carry-Adder circuit in Conventional CMOS using simple logic gates (not mirror circuit). Assume minimum L for all transistors. Assume that all inputs are coming from inverters with $W_n = 2L$ and $W_p = 2W_n$. Assume that all Sum outputs are connected to inverter loads of 100 times larger than the input inverters. The last Carry (only last one) is connected to inverter loads of 1000 times larger than the input inverters.

1. Design all other logic gates to be equivalent to twice the input inverters. Report the transistor diagram (not cadence), schematic view and simulation waveforms to show that they work properly for different data patterns. Measure the worst-case delay, energy dissipation, and static power, and estimate the area. Report the data in a table.

2. Find the capacitances at each node through Cadence and list in a table. Assuming equal signal probabilities of 0.5 for all inputs, estimate the energy dissipation using switching activity. Calculate switching activities for all nodes and list in a table with the total energy dissipation. Compare with *random pattern* simulations and comment.

3. Design all other logic gates (except for the input and output inverters) using the method of Logical Effort. Make sure that the last Sum delay is not more than Carry-out. Show your work and list all transistor sizes in a table. Implement the circuit and compare it delay, energy, and static power through simulations with case 1. Also estimate the area and compare to Part 1. Comment on results. Hint: You will get a system of equations that you should solve. One way is to assume some initial values and solve them by iterations until your values are only changing by 0.01 after each iteration.