Assignment 3, Due 29 March 2016

ELEC-5801: High-Speed and Low-Power VLSI

Department of Electronics, Carleton University

Maitham Shams

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1. Use the 65 nm CMOS technology kit with $V_{DD} = 1$ V . Implement the following 4-bit adder circuits: (a) Ripple-Carry-Adder using Conventional CMOS Mirror full-adder cells, (b) Carry-lookahead Adder, and (c) Carry-skip Adder. Size the logic gates to be equivalent to an inverter minimum L and $W_n = 2 \times L$ and $W_p = 5 \times L$. Report the transistor diagram, schematic view and simulation waveforms to show that they work properly for 10 different data patterns.

2. Measure the worst-case delay, maximum frequency of operation, static and dynamic power consumption at the highest frequency of operation, static and dynamic energy dissipations, and estimate the area for each case. Report the data in a table and comment on the comparison.