Assignment 2, Due 3 Mar 2016

ELEC-5801: High-Speed and Low-Power VLSI

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1. Use the 65 nm CMOS technology kit available to you. Connect N inverters of $W_n = 2 \times L$ and $W_p = (N/2 \ - \ 1/2) \times L$ in a closed loop. Assume that $IDLS$ is the least significant digit in your student ID. If $IDLS$ is odd, then $N = 4 + IDLS$, else $N = 5 + IDLS$. Use minimum L and typical $V_{DD} = 1\ V$ for the technology. Initialize the nodes to let the circuit oscillate. Report the schematic view and simulation waveform for any node. Measure the frequency of operation, dynamic power, and energy dissipations. Also report the value of the capacitance at any node. Then, open the loop and measure the total static power dissipation and the static power per inverter. Report these data in a clear table.

2. Use the technology parameters and your α-power law (from Assignment 1) and the capacitance values from Part 1 to calculate the frequency of operation for the circuit above. Also calculate the energy and power. Comment on the differences between your results and the simulations.

3. Keep W_p fixed and sweep W_n (from $0.5W_p$ to $2W_p$). Plot the frequency of operation versus $\beta = W_p/W_n$. Indicate for what value of β the frequency is maximum (this is β_{opt}). In a table compare the frequency, power, and energy for the circuit with the optimum β, to the original circuit in Part 1. How β_{opt} compare to $sqrtI_pIn$? Any comments?