Assignment 1, Due 28 January 2016

ELEC-5801: High-Speed and Low-Power VLSI

Department of Electronics, Carleton University

Maitham Shams

---

1. Use the 65 nm CMOS technology kit. For the PMOS and NMOS transistors, Plot I_D versus V_{GS} as V_{DS} changes and I_D versus V_{DS} as V_{GS} changes. Determine the saturation and linear regions and comment on the plots. In the 65 nm kit, there are High-V_t (hvt), Standard-V_t (svt), and Low-V_t (lvt) PMOS and NMOS devices. Consider all 6 cases. Let $L = L_{min}$ and $W = 130 + ID2$ (nm), where $ID2$ is the least two significent digits in you student ID.

2. For all PMOS and NMOS transistors find the parameters α and B for the MOSFET saturation current α-power law.

$$I_D = \frac{W}{L} B (V_{GS} - V_T)^{\alpha}$$

Form a table with these parameters. Plot I_D versus V_{GS} based on simulations and the model on the same graph and indicate the fitting points you used. comment on the results.