Sample Midterm Exam

MidDay, MidMonth, MidYear

ELEC4708: Advanced Digital Electronics

Department of Electronics, Carleton University

Instructor:	Maitham Shams	**Exam Duration:**	1 hour
Booklets:	None	**Number of Pages:**	4 with this
Aids Allowed:	Calculator	**Number of Students:**	MidNumber

Last Name: _____

First Name: _____

ID: _____

Q1	Q2	Q3	Q4	Total
/10	/5	/20	/15	/50

- Write your name and ID number clearly on all pages. No questions answered.
- Attempt all questions. Marking scheme for all questions are given.
- If in a question you are asked to make an assumption, then you must use it.
- Formula

$$\hat{D} = NF^{\frac{1}{N}} + P, \;\; F = GBH, \;\; \hat{f} = F^{\frac{1}{N}}, \;\; H = \frac{C_{out}}{C_{in}}$$

$$f = gh, \;\; b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}, \;\; G = \Pi g_i, \;\; P = \Sigma p_i$$

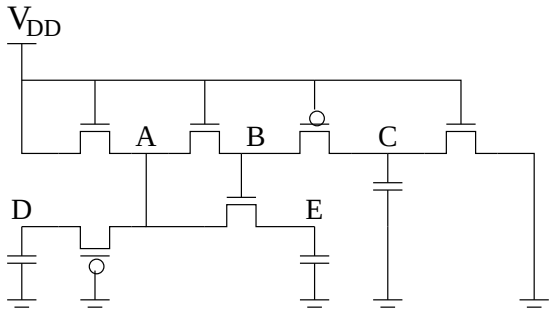
- Data

$$V_{DD} = 1.8 \text{ v}, V_{tn} = 0.4 \text{ v}, V_{tp} = 0.5 \text{ v}$$

[1] (10 marks, 1 marks each) Mark True or False.

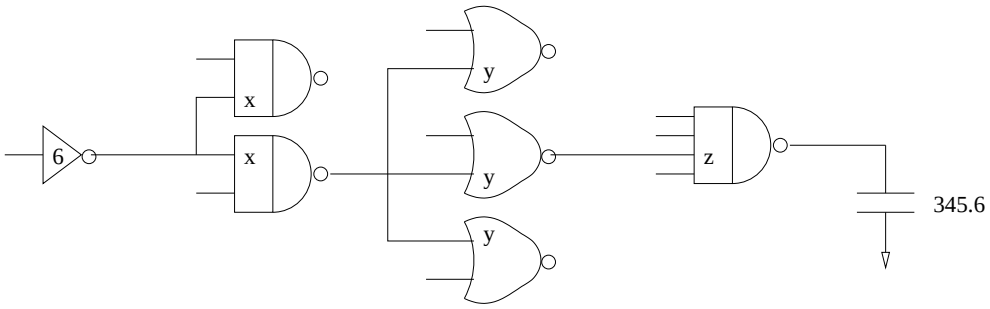
1. Body (substrate) of PMOS transistors are usually grounded. ☐ True ☐ False
2. A CMOS transmission gate consists of a PMOS and an NMOS transistor connected in parallel. ☐ True ☐ False
3. Stick diagrams may be used to estimate the area of logic gates. ☐ True ☐ False
4. Using only the true (not inverted) inputs, it is impossible to implement a CMOS non-inverting logic gate in one stage. ☐ True ☐ False
5. An ideal flip-flop is never transparent. ☐ True ☐ False
6. in modern CMOS IC technologies diffusion capacitances are much smaller than gate-oxide capacitances. ☐ True ☐ False
7. In modern CMOS digital circuits electron velocity doesn't saturate. ☐ True ☐ False
8. MOS threshold voltage is independent of source-body potential. ☐ True ☐ False
9. In modern CMOS digital circuits junction leakage current is less than subthreshold leakage current. ☐ True ☐ False
10. CMOS circuits operate faster at lower temperatures. ☐ True ☐ False

[2] (5 marks) Obtain the steady-state voltages at the nodes of the following circuit. All capacitances are 0.1 pF each and all the transistors have $W/L = 3$.



- $V_A =$
- $V_B =$
- $V_C =$
- $V_D =$
- $V_E =$

[3] (20 marks) Consider the following circuit. The inverter has an input capacitance of 6 units (i.e. twice as large as the unit inverter). The output capacitance is 345.6 units.



- Calculate the minimum possible delay for the circuit, if the delay of a unit inverter is 15 ps in this technology.

- Find the size of all unknown PMOS and NMOS transistors in the circuit.

[4] (15 marks) Implement the following function in conventional CMOS. Assume that both the true and inverted inputs are available. If there are more than one possible implementations, do the one that imposes less capacitive loas at the output, i.e., faster.

- $Z = \overline{A(B+C) + \bar{D}E}$

- Size the transistors such that the logic gate is equivalent (in resistance and current) to a unit inverter (i.e. $W_p/L_p = 2$ and $W_n/L_n = 1$). If there are more than one way of sizing, do the one that results in a faster circuit.

- If the output diffusion capacitance of a unit inverter is 12 fF, calculate the energy dissipation at the output Z.

- How much power do you save by operating with a power supply of 1.2 v instead of 1.8 v.