Lab 3
ELEC-4708: Advanced Digital Electronics
Automated Design, Synthesis, and Layout

In this lab you learn about designing an application circuit in CMOS, going from a functional description to the final layout (tape out). You are also going to verify the functionality of the design at different levels and measure the performance and power dissipation parameters that are important in digital design. You will be using the most advanced IC technology available to you and professional CAD tools. This experiment mimics the steps in a practical ASIC design. The text in italic indicates the deliverables.

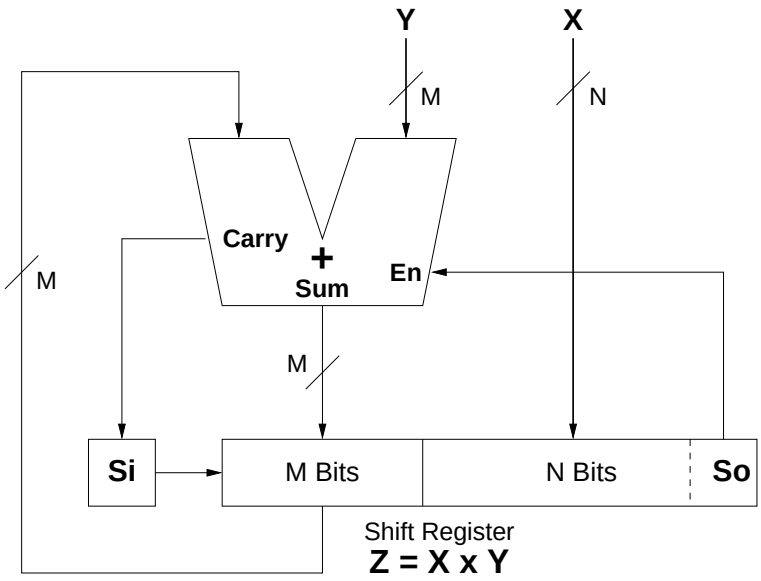

Figure 1: Unsigned Serial Multiplier

You will design a Signed Serial Multiplier. Figure 1 illustrates the structure of an unsigned serial multiplier circuit. It multiplies an N-bit multiplicant X with an M-bit multiplier Y and produces the $(M+N)$-bit product Z. It requires an MM-bit adder and an $(M+N)$-bit shift register. First, the shift register is loaded with X in the least significant N bits and zeros in the most significant M bits.The Shift-In bit (Si) is also reseted to 0. After that and in each cycle, the least significant bit of the shift register is checked. This bit is indicated as Shift-Out (So) in the figure. if So=1, then the full-adder is enabled and a copy of Y is added to the current most significant M bits of the shift register. The sum occupies the most significant M bits of the shift register and the carry (1 or 0) goes to Si. If So=0, no addition takes place. In both cases, the shift register is shifted right by one bit. This process is repeated for N clock cycles, when all bits of X have been checked and shifted out. Now, the shift register contains the final product Z.

The above procedure, however, only works for multiplying unsigned integers. To perform signed multiplication, the following steps must be added. First, take 2's complement of X, if it is negative. Second, take 2's complement of Y, if it is negative. Obviously to find out the sign of a variable, one checks its most significant bit; 1 indicates a negative sign and 0 indicates a positive sign. Finally, after the multiplication is done, takes 2's complement of Z, if the signs of X and Y are different.

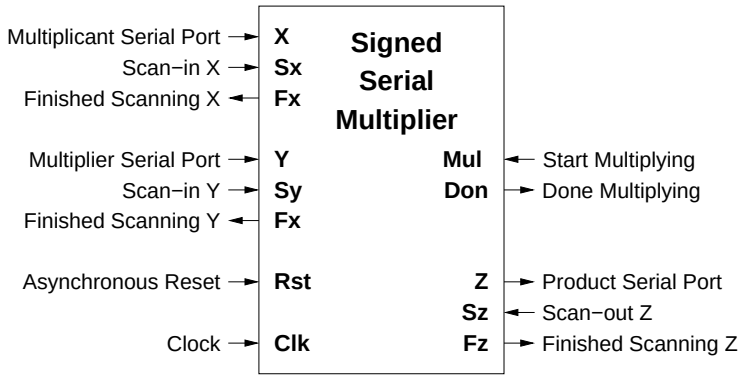

Figure 2: Pin Layout of the Unsigned Serial Multiplier

The pin layout of the multiplier is depicted in Figure 2. The multiplicant and the multiplier are scanned-in in a serial fashion and the product is scanned out similarly after the multiplication process is finished.

A: HDL Synthesis

Using an HDL, code the behaviour of the signed serial multiplier. Use the following formulas for obtaining M and N.

$$M = \text{Your ID's 1st least significant digit} + 8$$

$$N = \text{Your ID's 2nd least significant digit} + 8$$

Make a test bench and try the following test vectors.

1. 0×0
2. -1×-1
3. (largest positive X)/2 and (largest positive Y)/2
4. (largest negative X)/2 and (largest negative Y)/2
5. (largest positive X)/2 and (largest negative Y)/2
6. (largest negative X)/2 and (largest positive Y)/2
7. largest positive X and largest positive Y
8. largest negative X and largest negative Y

9. largest positive X and largest negative Y
10. largest negative X and largest positive Y

When you are sure that the code is working properly, synthesize the circuit.
[1]*Print a working copy of the code including detailed comments*.
[2]*Print a working copy of the test bench, test vectors and results*.
[3]*Estimate the maximum frequency of operation and the corresponding power dissipation*.
[4]*Print the synthesis report*.
[5]*Print the synthesized schematic*.

B: Automatic Layout and Tape out

Now, using the automated procedure, produce the chip layout.
[6]*Print the layout will cell placement only*.
[7]*Print the layout including cell placement, fill and routing*.
[8]*Print the full summary report*.
[9]*Print the terminal windows showing that you ran geometry and connectivity verifications*.
[10]*Print the verification browser output*.
[11]*Print the terminal window output for the GDS2 file including the layer names and numbers. What layers are missing?*
[12]*Why is it important to have a core utilization of less than one when designing the chip floor plan?*
[13]*Why the power-ring metal lines should be wide?*
[14]*Why do you normally need a clock tree?*
[15]*Why filler is added to the design?*
[16]*How many standard cells are used in your chip?*
[17]*Make a table that clearly includes all the important specifications of your final design and comment on where the information was found*.