Lab 1
ELEC-4708: Advanced Digital Electronics

CMOS Logic Schematic and Layout

In this lab you learn about designing a CMOS logic gate both at the schematic (Part A) and layout levels (Part B). You are also going to measure the various delay and power parameters that are important in digital design. You will be using the most advanced IC technology available to you. This lab runs for three weeks. The text in italic indicates the deliverables.

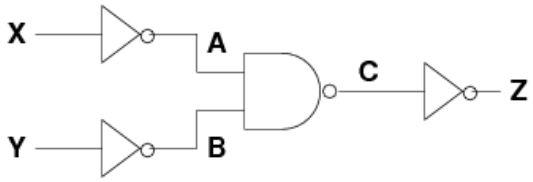
Deliverables

A: Schematic Entry

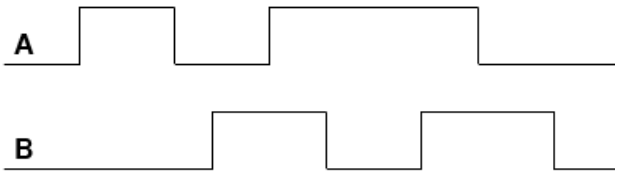
1. Implement a CMOS NAND gate. Let the length of all transistors be L nm, where L is the feature length or the minimum length allowable by the technology. Design the NAND gate such that its performance is equivalent to that of an inverter with PMOS to NMOS size ratio of $W_p/W_n = 2$. Use the two least significant digits in your user ID, id, to size the widths of the NMOS transistors according to the following formula.

$$W_n = 3L + id \text{ nm}$$

   Add inverter buffers to the inputs and outputs, as shown in the figure. Let $W_p/W_n = 2$ for all three inverters. For the input inverters make $W_n = 3L$ and for the output inverter make $W_n = 12L$. Use a different power supply for the NAND gate than the inverters (to help in measuring the power dissipation of the NAND gate). [1]*Print the schematics of the inverters, NAND gate, and testbench.*



Schematic Entry



Simulation Waveform

2. Use input waveforms to try all different combinations of inputs and their arrival sequences, i.e. A changing first and B changing first (the waveform shown in the figure should be sufficient). Make sure that the transitions are at least 1 ns apart from each other. [2]*Plot the waveforms A, B, and C.* [3]*Make a table of the rising and falling times, the propagation delays (maximum), and the contamination delays (minimum).* [4]*Explain which case gives you the largest and which case gives you the lowest delays.*

3. Now connect both inputs to a pulse wave. Sweep the input frequency from 250 MHz to 3 GHz in 250 MHz intervals. Measure the power dissipation of the NAND gate for each case. [5]*Plot the power dissipation versus frequency and calculate the total capacitance at node C.* [6]*Explain and justify the graph shape, and state when you think the circuit stops working.*

4. Sweep the size of the NAND gate by changing W_n from $3L$ to $20L$ in steps of $0.5L$ while keeping $W_p/W_n = 2$ (i.e. you may have to change W_p as well). Do not change the size of the inverters. Measure the average propagation delay from A (or B) to C in each case.

$$t_{pd} = (t_{pdr} + t_{pdf})/2$$

[7]*Plot the average propagation delay versus the size (W).* [8]*Explain and justify the graph shape, and indicate for what size the delay is optimum.*

B: Layout Entry

1. Implement a layout of only the NAND gate, with the sizes related to your ID as in step 1 of part A. [9] *Print your layout, LVS report, and DRC report.*

2. Extract the NAND gate with only capacitive parasitics. [10] *Explain why you are not concerned with the parasitic resistors?* [11] *Print the extracted view.*

3. Simulate the extracted view of the NAND gate in the same environment as before (the inverters should still be schematic view) [12] *Plot the waveforms.* [13] *Measure all the delay parameters again and list them in a table.* [14] *Compare the results with the purely schematic case.*