Sample Final Exam

FinalDay, FinalMonth, FinalYear

ELEC4708: Advanced Digital Electronics

Department of Electronics, Carleton University

Instructor:	Maitham Shams	**Exam Duration:**	3 hour
Booklets:	None	**Number of Pages:**	10 with this
Aids Allowed:	Calculator	**Number of Students:**	FinalNumber

Last Name: _____

First Name: _____

ID: _____

CANNOT BE TAKEN OUTSIDE EXAM AREA

Q1	Q2	Q3	Q4	Q5	Q6	Total
/30	/15	/15	/15	/10	/15	/100

- Write your name and ID number clearly on all pages. No questions answered.
- Attempt all questions. Marking scheme for all questions are given.
- If in a question you are asked to make an assumption, then you must use it.
- Formula

$$\hat{D} = NF^{\frac{1}{N}} + P, \;\; F = GBH, \;\; \hat{f} = F^{\frac{1}{N}}, \;\; H = \frac{C_{out}}{C_{in}}$$

$$f = gh, \;\; b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}, \;\; G = \Pi g_i, \;\; P = \Sigma p_i$$

- Data

$$V_{DD} = 1.8 \text{ v}, V_{tn} = 0.5 \text{ v}, V_{tp} = 0.5 \text{ v}$$

[1] (30 marks, 1 marks each) Mark True or False.

1. Carry-Select Adder uses double the hardware for calculating all SUM bits. ☐ True ☐ False
2. Carry Signal C_i is the group generate signal up to bit i (i.e. $G_{i:0}$). ☐ True ☐ False
3. Body (substrate) of NMOS transistors are usually grounded. ☐ True ☐ False
4. NMOS transistors are best in passing 1s. ☐ True ☐ False
5. Symmetric functions have similar pull-up and pull-down networks. ☐ True ☐ False
6. Purely combinational logic is impossible to be described inside an always block in Verilog. ☐ True ☐ False
7. Clock gating may produce false clock edges. ☐ True ☐ False
8. in modern CMOS IC technologies diffusion capacitances are much smaller than gate-oxide capacitances. ☐ True ☐ False
9. Last-arriving inputs should be connected to the transistors attached to the power rails (i.e. GND and V_{DD}). ☐ True ☐ False
10. In modern CMOS digital circuits electron velocity doesn't saturate. ☐ True ☐ False
11. MOS threshold voltage is independent of source-body potential. ☐ True ☐ False
12. A positive-edge-triggered flip-flop is transparent when clock is 1. ☐ True ☐ False
13. Ignoring the diffusion capacitances, the stage effeort for minimum delay is e. ☐ True ☐ False
14. In modern CMOS digital circuits junction leakage current is less than subthreshold leakage current. ☐ True ☐ False
15. Dynamic power dissipation increases linearly with frequency of operation. ☐ True ☐ False

16. A junction capacitance gets larger as the magnitude of the reverse-biased potential across the junction increases. ☐ True ☐ False
17. Fast multi-input adders are simply produced by cascading 2-input adders. ☐ True ☐ False
18. Delay of N serially connected MOSFETs increases quadratically with N. ☐ True ☐ False
19. CMOS circuits have higher static power dissipation at lower temperatures. ☐ True ☐ False
20. Leakage current through the gates of MOSFETS increases as the gate-oxide thickness reduces. ☐ True ☐ False
21. CVSL is a ratioless CMOS logic style. ☐ True ☐ False
22. The sharper the input signal, the higher the short-circuit current through a CMOS inverter. ☐ True ☐ False
23. A problem with Domino logic gates is that they are inherently non-inverting. ☐ True ☐ False
24. The major block in a subtractor circuit, is an adder. ☐ True ☐ False
25. CPL logic gates need a couple of PMOS transistors to produce full-swing outputs. ☐ True ☐ False
26. Static sequencing elemenets do not use clock signals, but dynamic sequencing elements do. ☐ True ☐ False
27. When comapring two signed numbers A and B, we know that A is larger than B, if $A - B$ produces a carry-out. ☐ True ☐ False
28. Regular latches should not be driven by brief pulses for sequencing. ☐ True ☐ False
29. Semidynamic flip-flops have static inputs and dynamic outputs. ☐ True ☐ False
30. The output of a symmetric function is inverted when all its inputs are inverted. ☐ True ☐ False

[2] (15 marks) Show the transistor-level implementations of 3-input XOR gate in Pseudo NMOS, conventional CMOS, CPL, and DCVSL (your book calls it CVSL), and single-rail (regular) Domino logic. Assume that inputs A, B, C and their complements are all available. Use minimum number of transistors in each case.

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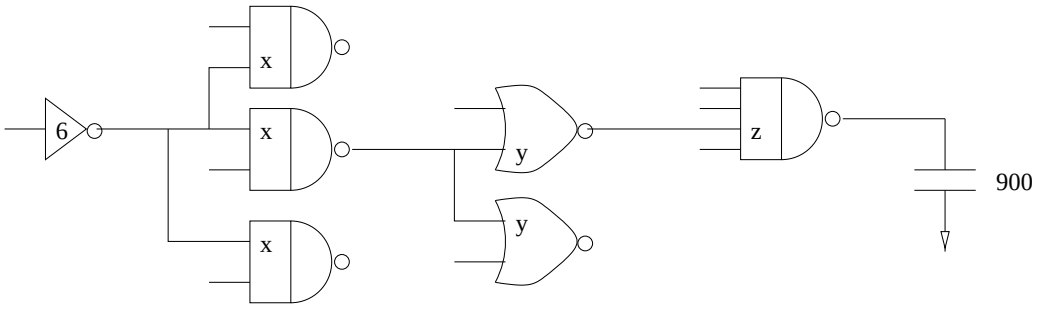
[3] (15 marks) Consider the following circuit. The inverter has an input capacitance of 6 units (i.e. twice as large as the unit inverter). The output capacitance is 900 units.



- What is the optimum number of stages for lowest delay? Modify (sketch) the circuit for minimum delay by adding inverters if necessary. Hint: Assume optimum stage effort is 4.
- Calculate the minimum possible delay for the original and modified circuit, if the delay of a unit inverter is 15 ps in the technology.
- Find the sizes of all unknown PMOS and NMOS transistors in the modified circuit.
- How does the delay of the modified circuit change if the power-supply voltage is reduced to 1.2 v from 1.8 v?

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[4] (15 marks) Sketch the block diagram and logic-gate level diagram of an 8-bit Carry-Lookahead Adder using valency-4 PG logic (two 4-bit adder blocks). Only use Inverters, two-input AND, OR, and XOR gates. Do not use any multi-input logic gates. Calculate the delay through the critical path, if the gate delays are: $t_i = 15$ ps (for INV), $t_a = 25$ ps (for AND), $t_o = 30$ ps (for OR), and $t_x = 40$ ps (for XOR), respectively.

[5] (10 marks) Draw the transistor-level circuit diagram of a positive-edge-triggered D-flipflop with synchronous set and reset control signals. Also draw the circuit diagram of one with asynchronous set and reset control signals. The inputs are D, ϕ, $\bar{\phi}$, $\overline{\text{set}}$, and $\overline{\text{reset}}$. The outputs are Q and $\bar{Q}$. The circuit diagram MUST show all transistors. You may start with logic-gate diagrams, then convert to transistor-level circuits.

[6] (15 marks) The Sum and Carry-Out of a full-adder cell are given by

$$S = A \oplus B \oplus C \qquad\qquad C_o = AB + AC + BC$$

The inputs A, B and C have 0.5, 0.5 and 0.25 probabilities of being 1, respectively. Find the power consumption for the Sum and Carry-Out output nodes. Assume that each of these outputs have a load capacitance of 100 fF and the circuit operates at 1 GHz. Ignore the internal node capacitances.