ELEC4708 Lab 2

Week 3: Automatic Layout

By this lab you should have finished synthesizing the Signed Multiplier. In this lab you will do automatic layout for the synthesized version of the Signed Multiplier using the First Encounter tool. Follow the instructions in the third tutorial for Automatic layout. **Make sure you answer the questions for part B while you are doing the tutorial.**

Signed multiplier Final Report:

Requirements:

- Do questions 1 to 17 in the overview instructions. They are repeated here for convenience. **Note: the questions asking for copies of code, waveforms, or schematics may be skipped if they have not changed since you last submitted them**. **However, you should leave a note at each respective question indicating that they were included in your previous report.**

Part A:

1. Print a working copy of the code including detailed comments.
2. Print a working copy of the test bench, test vectors and results.
3. Estimate the maximum frequency of operation and the corresponding power dissipation.
4. Print the synthesis report.
5. Print the synthesized schematic.

Part B:

6. Print the layout with cell placement only.
7. Print the layout including cell placement, fill and routing.
8. Print the full summary report.
9. Print the terminal windows showing that you ran geometry and connectivity verifications.
10. Print the verification browser output.
11. Print the terminal window output for the GDS2 file including the layer names and numbers. What layers are missing?
12. Why is it important to have a core utilization of less than one when designing the chip floor plan?
13. Why should the power-ring metal lines be wide?
14. Why do you normally need a clock tree?
15. Why is filler added to the design?
16. How many standard cells are used in your chip?
17. Make a table that clearly includes all the important specifications of your final design and comment on where the information was found.